FuturePlus Systems Corporation

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FS4410 SRIO State Analysis Probe User Manual

For use with Agilent Logic Analyzers

Revision – 1.6

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Due to the complex nature of the FS4410 and the wide variety of customer target implementations, the FS4410 has a 30 day acceptance period by the customer from the date of receipt. If the customer does not contact FuturePlus Systems within 30 days of the receipt of the product it will be said that the product has been accepted by the customer. If the customer is not satisfied with the FS4410 they may return the FS4410 within 30 days for a refund.

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Introduction

How to Use This Manual

This manual is organized to help you quickly find the information you need.

- **Analyzing the Serial Rapid IO bus** chapter introduces you to the FS4410 and lists the minimum equipment required and accessories supplied for Serial Rapid IO bus analysis.
- The **State Analysis** chapter explains how to configure the FS4410 to perform state analysis on your Serial Rapid IO bus.
- The **Transaction Viewer** chapter is a brief overview of this application software that integrates with the FS4410 Protocol Decoder. For more detail on it's operation refer to the FS1150 User manual on the FuturePlus Systems documentation CD.
- The **General Information** chapter provides information on the operating characteristics, and cable header pinout for the FS4410 probe.

Definitions

The following terms are used to describe aspects of the Serial Rapid IO (sRIO) bus:

- Channel - One differential signal (2 wires).
- sRIO Lane - A pair of differential signals running in opposite directions (4 wires).
- sRIO Link - A bidirectional interface made with two sets of unidirectional signals. A Link consists of 1, 2, 4, or 8 lanes.
- Link - One direction of a sRIO link. The FS4410 handles 1 or 2 links at a time, independently. This supports probing of both directions of a sRIO link, or probing of a pair of unrelated one-direction links. Links may be merged when displayed on the logic analyzer.
- Lane - One direction of a sRIO lane.

Analyzing the sRIO Bus

This chapter introduces you to the FS4410 probe and lists the minimum equipment required for sRIO bus analysis.

The FS4410 is a High Speed, Flexible Serial bus State Analysis probe. The probe is designed to handle two directions of a link, or a single direction from each of two unrelated links, using two link-processors (A and B), at lane widths of 1, or 4. The probe can connect to the sRIO target by a number of different means, including full and half-size midbus probes, or flying leads. The probe itself is controlled by the Probe Manager software, which runs under Windows and communicates with the probe via a USB cable.

The FS4410 probe "snoops" an sRIO link without significantly degrading its signal integrity. The high speed serial signal is deserialized and processed for packet identification by the probe before being sent to the logic analyzer connections. Additionally, the probe provides trigger, filtering, and packet recognition functions. The Protocol Decoder software running on the logic analyzer provides information regarding the transactions within the captured traffic, and the Transaction Viewer provides a system level view of these transactions.

Accessories Supplied

The FS4410 product consists of the following accessories:

- The FS4410 probe, power supply and cable, 16700 Protocol Decoder SW on floppy disk, 16900 Protocol Decoder, Probe Manager, and Transaction Viewer applications on CD. A USB cable is provided for connecting the FS4410 probe to the Windows based machine that the Probe Manager is loaded on.
- This operating manual on CD, Quick Start sheet, and SW Entitlement certificates for the FS4410 16700 Protocol Decoder and FS1134 16900/Offline Viewer.

Minimum Equipment Required

The minimum equipment required for analysis of a sRIO bus consists of the following equipment:

- Agilent 16700 analysis frame with the 1671x analyzer card or better. **To take advantage of all options, the 16753 or better cards are the preferred cards. Alternately, a 16900 frame and 16753/4/5/6 or 169xx cards can be used.**
- Revision 2.7 or better of the 167xx Agilent Logic analysis frame software.
- Revision 3.50.00 or better of the 169xx Agilent Logic analysis software
- An FS4410 probing cable
- A sRIO target bus. It is **STRONGLY recommended** that the user review and apply the probing guidelines described in the FuturePlus Systems application note "Logic Analyzer Probing Design Guide for the FS4410" when planning for use of the probe on any target system.

Probing System Overview

Several key elements of the FS4410 sRIO probing system and the target sRIO link architecture must be thoroughly understood before attempting to use the probe.

The following is a general outline of the steps to be taken when probing a new link. Read the following pages for more specific information.

The FS4410 probe requires the understanding and correct set-up of 4 different systems before a trace should be taken.

1. Probe Manager software. This software is identified as Probe Manager.exe and is on the CD that comes with the FS4410. Additionally, there is a folder within this CD that contains all the necessary USB drivers that your Windows system requires. When Windows searches for the USB drivers to load during the first connection of the FS4410, Windows **MUST be directed to load the drivers from this CD** in the system or the proper USB drivers will not load. In some cases it may necessary to temporarily disconnect the Windows system from the local network to insure that Windows does not automatically default to getting the drivers from the Internet. If the correct USB drivers are not loaded the user will see a Windows error ("Unable to load DLL") as soon as the "Run" button is used.

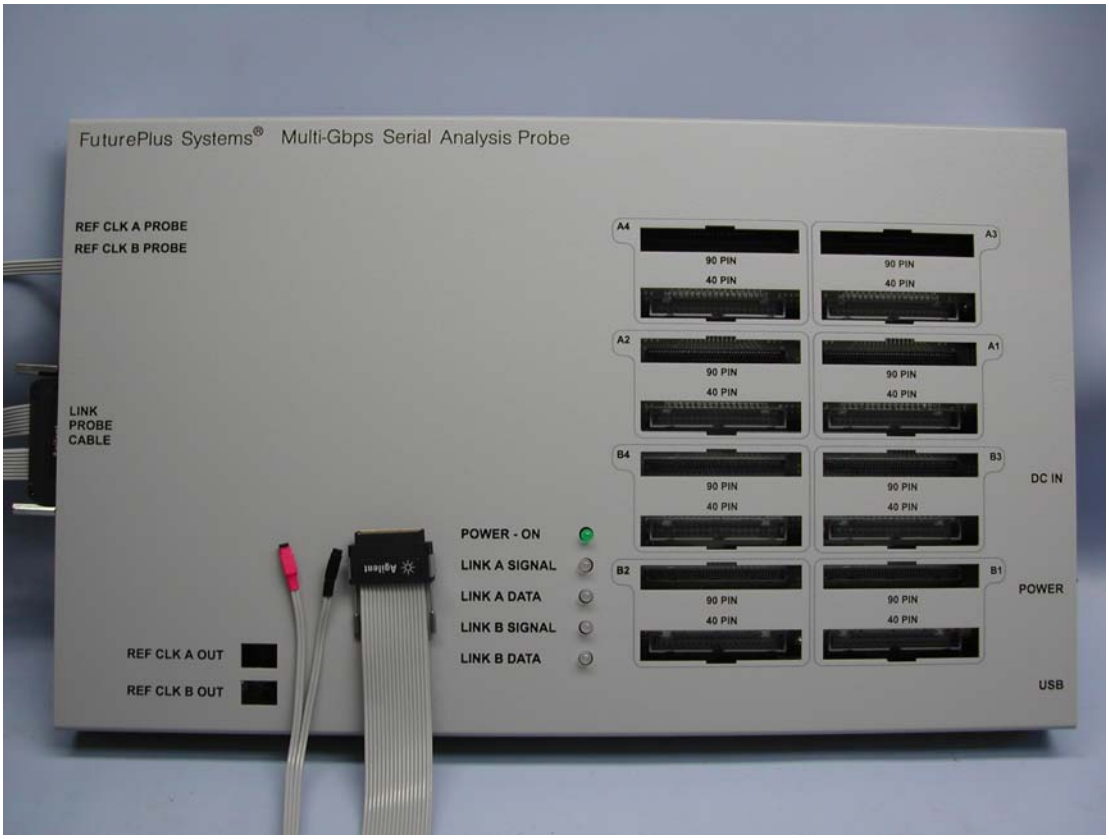
NOTE: The Microsoft .NET Framework must be on the system for the Probe Manager application to load properly.

2. FS4410 probe. This probing pre-processor requires its own DC power supply which is provided. Additionally, this probe is completely initialized, set-up and controlled by the Probe Manager software that resides on a Windows based system (PC or 1690x frame). All communication to the FS4410 probe is by means of the USB port on the PC (or 1690x frame). Improper or incomplete installation of either the correct USB driver or the Probe Manager software will prevent operation of the FS4410. If the target platform's transmitter frequency is not sRIO complaint (>100 ppm), then the probe will require an external reference clock connection to the target. The probe has a simple 4 LED display to indicate the status of the signal connection and acquired data.
3. Agilent Logic Analyzer. The configuration files and Protocol Decoder for the 1670x analyzers (FS4410) are on a diskette. The files for the 1690x analyzers (FS1134) are on a CD. Install these files as required and follow the instructions for logic analyzer module (card) interconnections and logic analyzer Pod connections to the FS4410 probe.
4. sRIO target platform. The target hardware must be prepared for probing per this document or the "sRIO Probing Logic Analyzer Probing Design Guide". For proper operation the Probe Manager must be set-up for the probe cable type and for the target system's sRIO attributes: lane width (1 or 4), speed grade (1, 2 or 3) and x1 x4 lane selection (0 or 2).

It is strongly recommended that the user methodically proceed in the following manner when setting up the probe. There is more detail on each step in this manual.

1. Load the Probe Manager software, configuration files and Protocol Decoder on the PC and/or 1690x logic analyzer. Leave the CD in the system for access to the USB drivers.
2. Configure (meld) the logic analyzer cards as required, remove any adapter cables on the Pod connections and run the Agilent Logic analyzer's internal diagnostics on the cards. If the analyzer passes then make the appropriate Pod connections to the FS4410 probe.
3. Connect the appropriate probing cable(s) to the target system, power up the probe. This may result in a Windows dialog searching for the "*FTDI FTD2XX*" USB drivers; direct it to the Probe Manager CD. Check the Windows Device Manager to make sure that it loaded properly.
4. Open up the Probe Manager application and select the appropriate settings for the probe cable being used and the sRIO link. Prior to running the probe, check that the activity indicators (up and down arrows) are displayed in the proper lanes. For the first logic analyzer capture, turn off all the filters.
5. Run the probe. Check that the Link A and B signal and data LEDs are green. Trigger the logic analyzer and examine the captured trace file. If it has no error messages then it is a good indication that all initial settings are correct.

Front Panel



The connections and features of the FS4410 probe include:

- DC input for provided external AC to DC power supply (please note that the use of any other power supply voids the warranty on the FS4410), On/Off switch and USB connections to the Windows PC/16900 where the Probe Manager software will be loaded.
- Link Probe cable connection for any 1 of 3 different probing cables and Reference Clock probe cable connections.
- Logic Analyzer probe connections. One set for 90 pin pod connections and a duplicate set for 40 pin pod connections. A1 – A4 are connections for 1 Link Processor, and B1 – B4 are for the other Link Processor.
- Reference Clock Probe Cable is permanently attached to the FS4410.
- LED indication of probe power on and Link status. For each link there is a pair of LEDs which have the following states:

Link A or B Signal LED color	Meaning
Green	Link OK
Dark	Loss of Signal
Orange	Data Invalid (8b10b error)
Red	Receiver Fault

Link A or B Data LED color	Meaning
Green	Data clocking Into Analyzer
Dark	No Data clocking into Analyzer
Orange	Any Error: 8b10b, Align, Framing, Idle
Red	Processor Clock Error

FS4410 Probing Cables

The FS4410 sRIO probe can be configured with a wide variety of different probing cables dependent on what the user requires:

FS1031 Full size midbus footprint probe cable

FS1032 ½ size midbus footprint probe cable

FS1036 Flying lead probing cable

The “sRIO Probing Design Guide for the FS4410” provides specific information on the successful application of midbus probing and also details general requirements for the Reference Clock signal and other aspects of the link to be probed. The FS4410 manual assumes that the user is familiar with this information and has applied it.

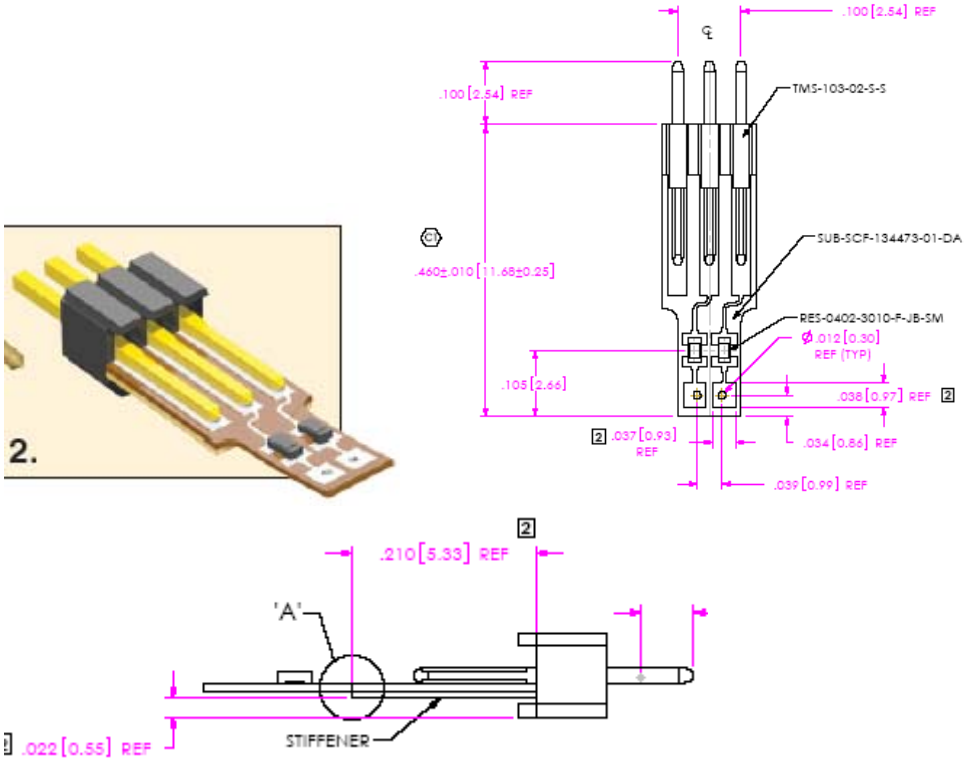
The probe cable should be attached to the FS4410 and carefully secured with the 2 captive fasteners on the cable. The probing end should be attached to the target either by screwing into the retention module (midbus probe) or sliding the flying lead probes onto the special resistors (see next section).

Note that the external Reference Clock is required when:

- The target transmitter frequency is not within 100 ppm of nominal.
- Link transmitter frequency is other than 1.25, 2.5, or 3.125 Gbps.
- Probe is being operated in 10-bit Mode.

Flying Lead Probing (FS1036 cable assembly)

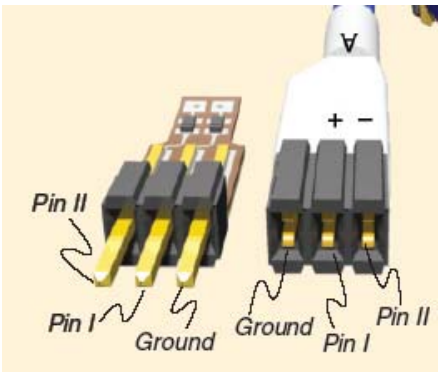
The FS1036 flying lead cable assembly allows the FS4400 probe to connect to components on the target board by means of directly soldering a flex pcb to a component or feature on the target pcb, then connecting the header on the flying lead cable to the other end of the flex pcb.



A few general guidelines about the use of the flying lead cable

1. There is an instruction booklet with the FS1036 cable that provides detail on how to solder the flex pcb to your board. Refer to this document.

2. Polarity matters. Makes sure you know how the + and – sides of the signal are connected. Adjustment to polarity can be made in the Probe manager.



The FS1036 flying lead cable has 8 pairs of channel connectors which are labeled A-G for up to 4 channels of a link and B-H which can be used for another link.

Make the appropriate cable and channel selections in the Probe manager before taking any probe measurements.

Installing your Software for the First Time

The following outlines the software installation procedure when using the probe for the first time. Please do not attach the probe to the analyzer or computer that will be controlling the probe until told to do so.

1. Place the software CD that came with the product into the logic analyzer or computer that you will be installing the software on.
2. Navigate to the installation CD using Windows explorer and click on the following files. Follow the instructions on the screen to install.*
   - FS1134.exe
   - FS1150.exe
   - Probe Manager.exe
3. Once all the above files have been installed, connect the FS4410 to the analyzer/computer via the USB port. Power on the FS4410 probe.
4. The found new hardware wizard should appear the first time the probe is attached and powered up. Select “no, not this time” when it asks if the computer can go to Windows update to search for the software. Then select next.
5. On the next screen select the advanced option (not the recommended) to select from a specific list or location. Select next.
6. Select the CD-ROM drive to load the driver from; you do not have to select a specific directory. Select next.
7. There may be a warning that comes up about Windows XP compatibility, ignore this warning and continue with installation.
8. Click finish to complete the installation.

Once all the previous steps have completed all necessary software as well as USB drivers will be installed. This procedure only needs to be done on initial install. You may now go to the desktop and click on the Probe manager icon to start the probe manager.

*If you are installing on a PC to only control the FS4410 probe then you can omit the installation of the FS1134.exe and FS1150.exe, but you must follow the rest of the steps.

For instructions on loading configuration files please refer to the section on loading configuration files later in this manual.

Connecting the Agilent logic analyzer to the FS4410

The FS4410 is designed to enable the user to connect the FS4410 to the widest possible range of Agilent logic analyzer modules (cards). This table describes the possible configurations:

Module PN	16900 or 16700 frame	Module quantity for X1 sRIO 1.25 Gbps (State Clock 63MHz)	Module quantity for X1 sRIO 2.5 Gbps (State Clock 125 MHz)	Module quantity for X1 sRIO 3.125 Gbps (State Clock 157 MHz)	Module quantity for X4 sRIO 1.25 Gbps (State Clock 125 MHz)	Module quantity for X4 sRIO 2.5 Gbps (State Clock 250 MHz)	Module quantity for X4 sRIO 3.125 Gbps (State Clock 313 MHz)
16950	16900	2 cards	2 cards	2 cards	2 cards	2 cards	2 cards
16911	16900	2 cards	2 cards	2 cards	2 cards	2 cards	4 cards
16910	16900	2 cards	2 cards	2 cards	2 cards	2 cards	2 cards
16753-6	Both	2 cards	2 cards	2 cards	2 cards	2 cards	2 cards
16760	Both	4 cards	4 cards	N/A	4 cards	N/A	N/A
16750-2	Both	2 cards	2 cards	2 cards	2 cards	4 cards	4 cards
16740-2	Both	2 cards	2 cards	2 cards	2 cards	N/A	N/A
16717-9	16700	2 cards	2 cards	2 cards	2 cards	4 cards	4 cards
1680/90	Alone	8/1 pods	8 pods	8 pods	8 pods	N/A	N/A
1680x	Alone	8/1 pods	8 pods	8 pods	8 pods	8 pods	N/A

For the 16900 Logic Analyzer

Use the General Purpose Probe feature in the Overview section of the 16900 Logic Analyzer application to connect the logic analyzer cables to the FS4410 probe.

For the 16700 Logic Analyzer

Connect the logic analysis cards to the FS4410.

Logic Analyzer	FS4410	Comment
Master Pod 1	A1	J clock A link
Master Pod 2	A2	
Master Pod 3	A3	
Master Pod 4	A4	
Expander Pod 1	B1	J clock B link
Expander Pod 2	B2	
Expander Pod 3	B3	
Expander Pod 4	B4	

Based on the probing needs install the appropriate modules into the Agilent logic analyzer and remove any adapter cables that may be attached to the module cables. When probing 2 directions of x1, or x4 links, the FS4410 drives 8 pods of signals to the logic analyzer. When probing a single direction of a x1 or x4 link, the FS4410 drives 4 pods of signals to the logic analyzer.

For probing a single direction of a link, a single machine is used. For probing two directions of a link, two machines are used. A state clock is provided to each machine and the frequencies may differ slightly.

It is important before you load a configuration file you initiate a self test on all your modules installed in your logic analyzer to insure all modules are working properly.

Setting up the 167xx Analyzer

For 167XX logic analyzer installations, the FS4410 software consists of one diskette.

To install the FS4410 software, insert the diskette labeled 16700/702 Installation disk for the FS4410 into the Agilent 1670x diskette drive. From the SYSTEM ADMINISTRATION TOOLS select INSTALL under SOFTWARE. From the SOFTWARE INSTALL screen select the FLEXIBLE DISK and APPLY. Once the title appears select it and then select INSTALL.

This procedure does not need to be repeated. It only needs to be done the first time the FS4410 sRIO State Analysis Probe is used.

When this has completed, load the appropriate configuration file from the /configs/FuturePlus/FS4410 directory. Refer to the table on the following pages for a list of analyzers and corresponding configuration files.

Setting up the 169xx Analyzer

The 16900 Analyzer is a PC based application that requires a PC running the Windows OS with the Agilent logic analyzer software installed or a 169xx frame.

Before installing the protocol decoder for the FS4410 on a PC you **must** install the Agilent logic analyzer software first. Once the Agilent logic analyzer software is installed, you can install the FS4410 protocol decoder by placing the CD-ROM disk into the CD-ROM drive of the target computer or Analyzer and executing the .exe setup program that is contained on the disk. The .exe setup file can be executed from within the File Explorer PC Utility. You must navigate to the FS1134.exe file on the CD-ROM disk and then double click the FS1134.exe file from within the File Explorer navigation panel.

The installation procedure does not need to be repeated. It only needs to be done the first time the Analysis Probe is used.

169xx Licensing

The FS4410 Protocol Decoder is a licensed product that is locked to a single hard drive. The licensing process is performed by Agilent. There are instructions on this process on the SW Entitlement certificate provided with this product.

Loading 1680/90/900 configuration files

When the software has been licensed you should be ready to load a configuration file. You can access the configuration files by clicking on the folder that was placed on the desktop. When you click on the folder it should open up to display all the configuration files to choose from. If you put your mouse cursor on the name of the file a description will appear telling you what the setup consists of, once you choose the configuration file that is appropriate for your configuration the 16900 operating system should execute. The protocol decoder automatically loads when the configuration file is loaded. If the decoder does not load, you may load it by selecting tools from the menu bar at the top of the screen and select the decoder from the list.

Configuration Files

The analyzers supported by the FS4410 configuration files are for the 16717 or better on the 16700/702 frames. 16753 and better analyzer cards are recommended.

8b mode only

167xx Analyzer	169xx Analyzer	X1 2 way any cable Any link speed		X4 2 way using any cable 1.25		2.5		3.125 Gbs	
		1 way	2 way	1 way	2 way	1 way	2 way	1 way	2 way
16715/6/7 or 16750/1/2		SR441_1	load twice	SR441_1	load twice	SR441_3	load twice	SR441_3	load twice
	16750/1/2, 16910/1	SR441_11	SR441_12	SR441_11	SR441_12	SR441_13	SR441_14	SR441_13	SR441_14
16753-6		SR441_5	load twice	SR441_5	load twice	SR441_5	load twice	SR441_5	load twice
	16753-6 or 1695x	SR441_15	SR441_16	SR441_15	SR441_16	SR441_15	SR441_16	SR441_15	SR441_16
16760		SR441_9	load twice	SR441_9	load twice	na	na	na	na
	16760	SR441_19	SR441_19	SR441_19	SR441_19	na	na	na	na
16740/1/2		SR441_1	load twice	SR441_1	load twice	na	na	na	na
	16740/1/2	SR441_11	SR441_12	SR441_11	SR441_12	na	na	na	na
1680x		SR441_50	SR441_51	SR441_50	SR441_51	SR441_50	SR441_51	na	na
1680/90 (Standalone)		SR441_21	SR441_22	SR441_21	SR441_22	na	na	na	na

SR441_1 – 1 way consists of 1 logic analyzer card.

SR441_3 – 1 way consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

SR441_4 – 2 way, consists of a total of 4 cards, each analyzer consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

SR441_5 – 1 way consists of 1 logic analyzer card.

SR441_6 – 2 way consists of 2 separate logic analyzer cards.

SR441_9 – 1 way consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode. 1 way consists of 1 logic analyzer card.

SR441_11 – 1 way consists of 1 logic analyzer card.

SR441_12 – 2 way consists of 2 separate logic analyzer cards.

SR441_13 – 1 way consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

SR441_14 – 2 way, consists of a total of 4 cards, each analyzer consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

SR441_15 – 1 way consists of 1 logic analyzer card.

SR441_16 – 2 way consists of 2 separate logic analyzer cards.

SR441_19 – 1 way consists of 2 logic analyzer cards configured as 1 analyzer running in turbo mode.

SR441_21 – 1 way, 1680/90 (Standalone)

SR441_22 – 2 way, 1680/90 (Standalone)

SR441_50 – 1 way, 1680x requires 4 pods

SR441_51 – 2 way, 1680x requires 8 pods

Connecting the Agilent logic analyzer to the FS4410 in 10b Mode

Module PN	16900 or 16700 frame	Module quantity for 10b mode X1 sRIO 1.25 Gbps (State Clock 125MHz)	Module quantity for 10b mode X1 sRIO 2.5 Gbps (State Clock 250 MHz)	Module quantity for 10b mode X1 sRIO 3.125 Gbps (State Clock 313 MHz)	Module quantity for 10b mode X4 sRIO 1.25 Gbps (State Clock 125 MHz)	Module quantity for 10b mode X4 sRIO 2.5 Gbps (State Clock 250 MHz)	Module quantity for 10b mode X4 sRIO 3.125 Gbps (State Clock 313 MHz)
16950	16900	2 cards	2 cards	2 cards	2 cards	2 cards	2 cards
16911	16900	2 cards	2 cards	2 cards	2 cards	2 cards	4 cards
16910	16900	2 cards	2 cards	2 cards	2 cards	2 cards	2 cards
16753-6	Both	2 cards	2 cards	2 cards	2 cards	2 cards	2 cards
16760	Both	4 cards	4 cards	N/A	4 cards	N/A	N/A
16750-2	Both	2 cards	2 cards	2 cards	2 cards	4 cards	4 cards
16740-2	Both	2 cards	N/A	N/A	2 cards	N/A	N/A
16717-9	16700	2 cards	2 cards	2 cards	2 cards	4 cards	4 cards
1680/90	Alone	8/1 pods	N/A	N/A	8 pods	N/A	N/A
1680x	Alone	8/1 pods	8 pods	8 pods	8 pods	8 pods	N/A

Configuration Files for 10b Mode

167xx Analyzer	169xx Analyzer	sRIO X4 10b mode link spd 1.25 Gbps 1 way	2 way	sRIO X4 10b mode link spd 2.5 Gbps 1 way	2 way	sRIO X4 10b mode link spd 3.125 Gbps 1 way	2 way
16715/6/7 or 16750/1/2		SR10b_16	load twice	SR10b_17	load twice	SR10b_17	load twice
	16750/2, 16910/1	SR10b_1	SR10b _2	SR10b_3	SR10b_4	SR10b_3	SR10b_4
16753-6		SR10b_18	load twice	SR10b_18	load twice	SR10b_18	load twice
	16753-6 or 1695x	SR10b_5	SR10b_6	SR10b_5	SR10b_6	SR10b_5	SR10b_6
16760		SR10b_19	load twice	SR10b_20	N/A	SR10b_20	N/A
	16760	SR10b_7		SR10b_8	N/A	SR10b_8	N/A
	16740/1/2	SR10b_1	SR10b _2	N/A	N/A	N/A	
	1680/90	SR10b_9	SR10b_10	N/A	N/A	N/A	
	1680x	SR10B_50	SR10B_51	PB10B_50	SR10B_51	SR10B_52	N/A

SR10b_1 – 1 way, x4 link, 1 analyzers, 40 pin connector cards

SR10b_2 – 2 way, x4 link, 2 analyzers, 40 pin connector cards

SR10b_3 – 1 way, x4 link, 2 analyzer cards, 40 pin connector cards

SR10b_4 – 2 way, x4 link, 4 analyzer cards, 2 analyzers, 40 pin connector cards

SR10b_5 – 1 way, x4 link, 1 analyzer, 90 pin connector card

SR10b_6 – 2 way, x4 link, 2 analyzer cards, 2 analyzers, 90 pin connector cards

SR10b_7 – 1 way, x4 link, 2 analyzer cards, 90 pin connector cards

SR10b_8 – 1 way, x4 link, 2 analyzer cards, 90 pin connector cards

SR10B_9 – 1 way, x4 link. 1 analyzer, standalone

SR10b_10 – 2 way, x4 link. 2 analyzers, standalone split analyzer.

SR10b_16 – 1 way, x4 link, 1 analyzer, for 2 way load twice, needs 2 cards

SR10b_17 – 1 way, x4 link, 1 analyzer, 2 cards. for 2 way load twice, needs 4 cards

SR10b_18 – 1 way, x4 link, 1 analyzer. Load twice for 2 way, need 2 cards.

SR10b_19 – 1 way, x4 link, 1 analyzer, 2 cards.

SR10b_20 – 1 way, x4 link, 2 analyzers, 3 cards.

SR10b_50 – 1 way, x4 link. 1 analyzer

SR10b_51– 1 way, x4 link. 2 analyzers

SR10B_52 – 2 way, x4 link. 1680x analyzer, split machine.

167xx Analyzer	169xx Analyzer	sRIO X1 10b mode link spd 1.25 Gbps		sRIO X1 10b mode link spd 2.5 Gbps		sRIO X1 10b mode link spd 3.125 Gbps	
		1 way	2 way	1 way	2 way	1 way	2 way
16715/6/7 or 16750/1/2		SR10b_11	load twice	SR10b_12	load twice	SR10b_12	load twice
	1675x, 16910/1	SR10b_11	SR10b_12	SR10b_11	SR10b_12	SR10b_11	SR10b_12
16753-6		SR10b_13	load twice	SR10b_13	load twice	SR10b_13	load twice
	16753-6 or 1695x	SR10b_13	SR10b_14	SR10b_13	SR10b_14	SR10b_13	SR10b_14
16760		SR10b_14	load twice	SR10b_14	load twice	SR10b_14	load twice
	16760	SR10b_15	SR10b_16	SR10b_15	SR10b_16	SR10b_15	SR10b_16
	16740/1/2	SR10b_18	SR10b_19	N/A	N/A	N/A	
	1680/90	SR10b_20	SR10b_21	N/A	N/A	N/A	
	1680x	SR10b_53	SR10b_54	SR10b_53	SR10b_54	SR10b_53	N/A

SR10b_11 – 1 way, x1 link, 1 analyzer, 40 pin connector cards.

(167xx Analyzer)**SR10b_12** – 1 way, x1 link, 1 analyzer, 2 analyzers, 2 cards for 2 way

SR10b_12 – 2 way, x1 link, 2 analyzer, 40 pin connector cards.

SR10B_13 – 1 way, x1 link, 1 analyzer, 90 pin connector cards.

(167xx Analyzer)**SR10B_14** – 1 way, x1 link, 1 analyzer, 2 cards, 2 analyzers for 2 way

SR10b_14 – 2 way, x1 link, 2 analyzers, 90 pin connector cards.

SR10b_15 – 1 way, x1 link. 1 analyzer, 90 pin connector cards.

SR10b_16 – 1 way, x1 link. 2 analyzers, 90 pin connector cards.

SR10b_18 – 1 way, x1 link, 1 analyzer, 40 pin connector card.

SR10b_19 – 2 way, x1 link, 2 cards, 2 analyzers, 40 connector card.

SR10b_20 – 1 way, x1 link, 1 analyzer, standalone

SR10b_21 – 2 way, x1 link, 2 analyzers, standalone split analyzer

SR10b_53 – 1 way, x1 link, 1 analyzer

SR10b_54 – 2 way, x1 link, 2 analyzers, 1680x analyzer, split machine

Offline Analysis

Data that is saved on a 167xx analyzer in fast binary format, or 16900 analyzer data saved as a *.ala file, can be imported into the 1680/90/900 environment for analysis. You can do offline analysis on a PC if you have the 1680/90/900 operating system installed on the PC, if you need this software please contact Agilent.

Offline analysis allows a user to be able to analyze a trace offline at a PC so it frees up the analyzer for another person to use the analyzer to capture data.

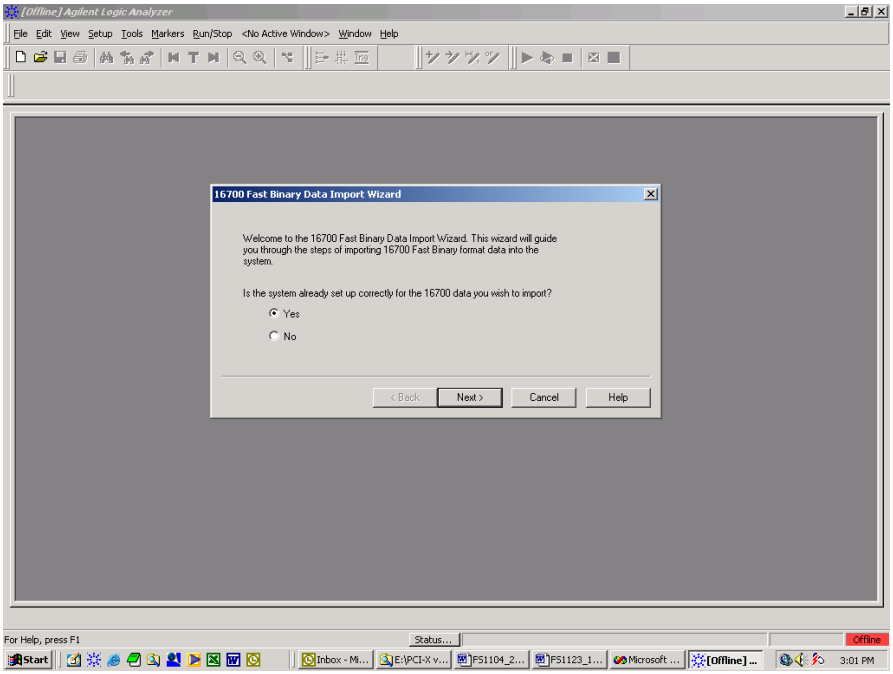
If you have already used the license that was included with your package on a 1680/90/900 analyzer and would like to have the offline analysis feature on a PC you may get additional licenses at no charge, please contact FuturePlus.

In order to view decoded data offline, after installing the 1680/90/900 operating system on a PC, you must install the FuturePlus software. Please follow the installation instructions for “Setting up 1680/90/900 analyzer”. Once the FuturePlus software has been installed and licensed follow these steps to import the data and view it.

From the desktop, double click on the Agilent logic analyzer icon. When the application comes up there will be a series of questions, answer the first question asking which startup option to use, select Continue Offline. On the analyzer type question, select Cancel. When the application comes all the way up you should have a blank screen with a menu bar and tool bar at the top.

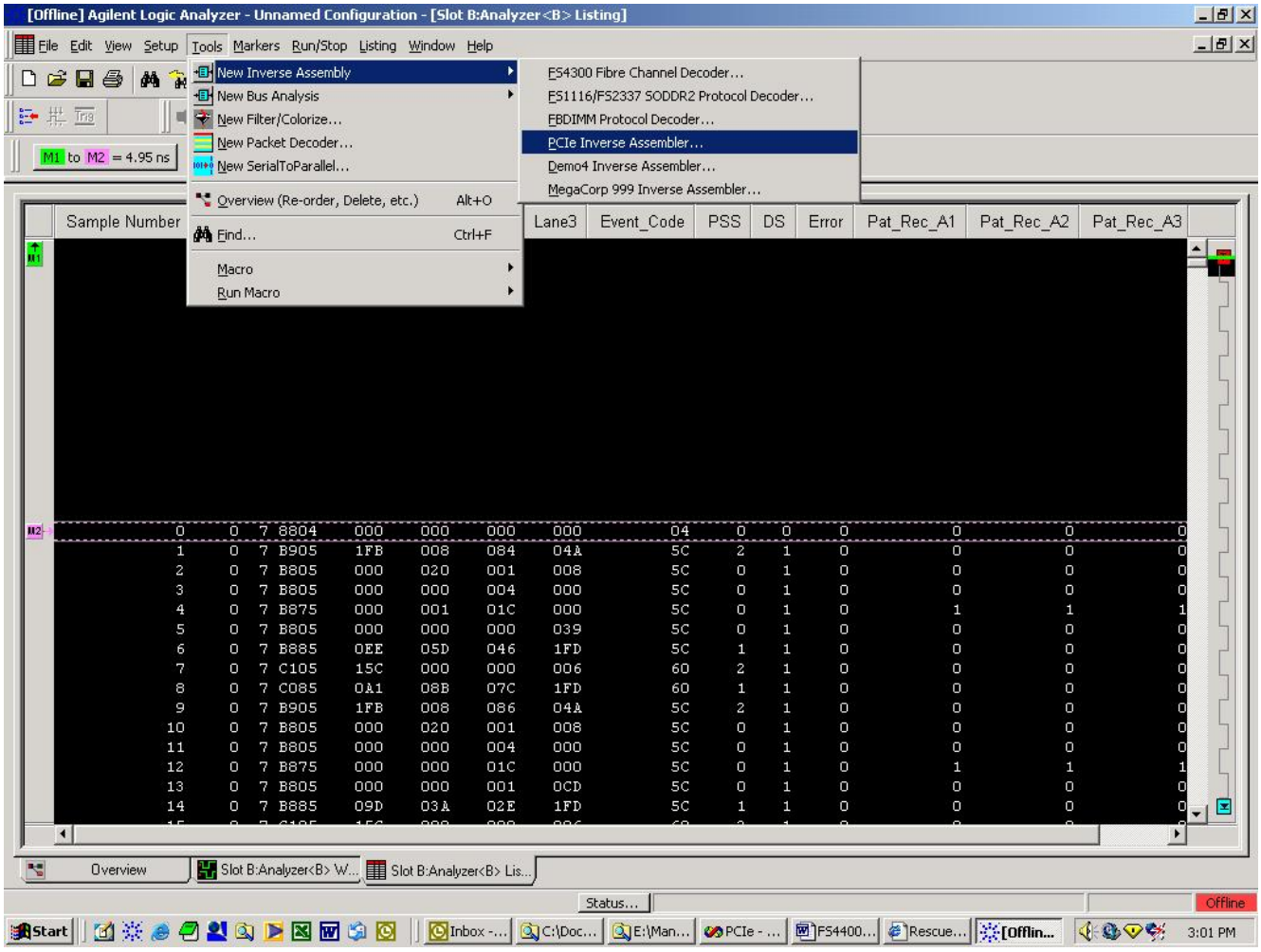
For data from a 1680/90/900 analyzer, open the .ala file using the File, Open menu selections and browse to the desired .ala file.

For data from a 16700, choose File -> Import from the menu bar, after selecting import select “yes” when it asks if the system is ready to import 16700 data.


[Offline] Agilent Logic Analyzer
File Edit View Setup Tools Markers Run/Stop <No Active Window> Window Help
16700 Fast Binary Data Import Wizard
Welcome to the 16700 Fast Binary Data Import Wizard. This wizard will guide you through the steps of importing 16700 Fast Binary format data into the system.
Is the system already set up correctly for the 16700 data you wish to import?
Yes
No
< Back
Next >
Cancel
Help
For Help, press F1
Status...
Offline
Start
3:01 PM

After clicking “next” you must browse for the fast binary data file you want to import. Once you have located the file and clicked start import, the data should appear in the listing.

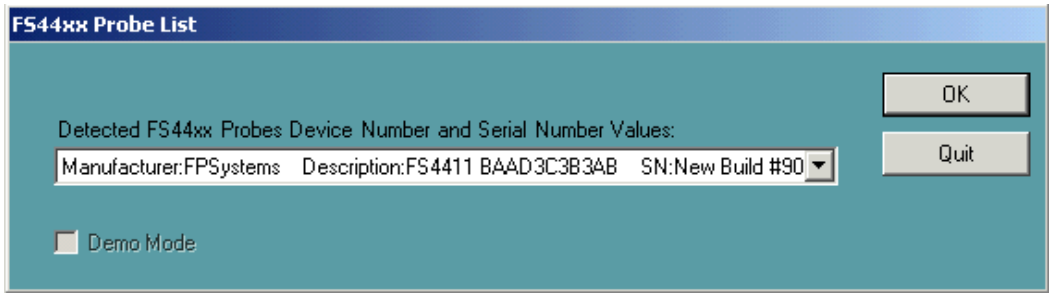
After the data has been imported you must load the protocol decoder before you will see any decoding. To load the decoder select Tools from the menu bar, when the drop down menu appears select Inverse Assembler, then choose the name of the decoder for your particular product. The figure below is a general picture; please choose the appropriate decoder for the trace you are working with.


[Offline] Agilent Logic Analyzer - Unnamed Configuration - [Slot B:Analyzer<B> Listing]
File Edit View Setup Tools Markers Run/Stop Listing Window Help
New Inverse Assembly
New Bus Analysis
New Filter/Colorize...
New Packet Decoder...
New SerialToParallel...
Overview (Re-order, Delete, etc.) Alt+O
Find... Ctrl+F
Macro
Run Macro
FS4300 Fibre Channel Decoder...
FS1116/FS2337 SODDR2 Protocol Decoder...
FBDIMM Protocol Decoder...
PCIe Inverse Assembler...
Demo4 Inverse Assembler...
MegaCorp 999 Inverse Assembler...
M1 to M2 = 4.95 ns
Sample Number
Lane3 Event_Code PSS DS Error Pat_Rec_A1 Pat_Rec_A2 Pat_Rec_A3
0 0 7 B804 000 000 000 000 04 0 0 0 0 0 0
1 0 7 B905 1FB 008 084 04A 5C 2 1 0 0 0 0
2 0 7 B805 000 020 001 008 5C 0 1 0 0 0 0
3 0 7 B805 000 000 004 000 5C 0 1 0 0 0 0
4 0 7 B875 000 001 01C 000 5C 0 1 0 1 1 1
5 0 7 B805 000 000 000 039 5C 0 1 0 0 0 0
6 0 7 B885 0EE 05D 046 1FD 5C 1 1 0 0 0 0
7 0 7 C105 15C 000 000 006 60 2 1 0 0 0 0
8 0 7 C085 0A1 08B 07C 1FD 60 1 1 0 0 0 0
9 0 7 B905 1FB 008 086 04A 5C 2 1 0 0 0 0
10 0 7 B805 000 020 001 008 5C 0 1 0 0 0 0
11 0 7 B805 000 000 004 000 5C 0 1 0 0 0 0
12 0 7 B875 000 000 01C 000 5C 0 1 0 1 1 1
13 0 7 B805 000 000 001 0CD 5C 0 1 0 0 0 0
14 0 7 B885 09D 03A 02E 1FD 5C 1 1 0 0 0 0
Overview
Slot B:Analyzer<B> W...
Slot B:Analyzer<B> Lis...
Status...
Offline
Start
Inbox -...
C:\Doc...
E:\Man...
PCIe - ...
FS4400...
Rescue...
[Offlin...
3:01 PM

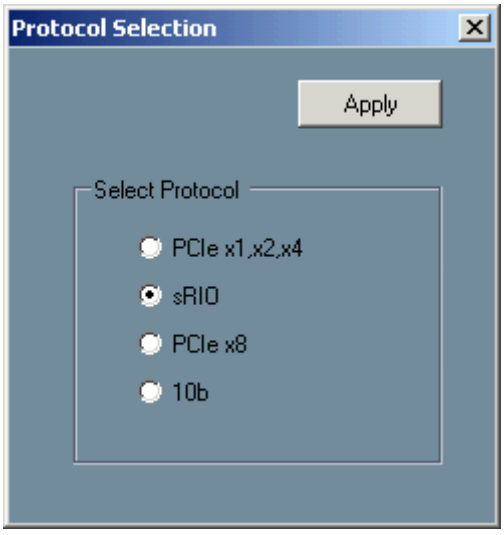
Probe Manager Application

The Probe Manager software can be found as the FS4410_probe_setup.exe file on the CD provided in the Documentation package. Insert the CD into the computer that will be used to control the FS4410 probe. This computer must have a USB connection. Using Windows File Manager, select the FS4410_probe_setup.exe file and double-click it, which initiates the installation software on the computer and places an icon on the desktop. Follow the directions that follow including agreeing to the license terms, once the software installation is complete click on finish. To start the program manager simply double click the FS4410 icon that is placed on the desktop.

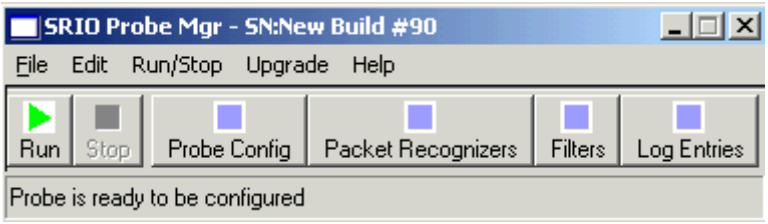
The Probe Manager application detects all FS44xx probes that are connected to the USB bus and allows the user to select which probe will be controlled by the current instance of the Probe Manager application from the initial screen as seen below.



The initial screen is followed by the Protocol Selection screen, in which the user selects the protocol the FS4410 probe will be associated with.



Once the protocol has been selected, the application displays the Main dialog as seen below.



The user configures and controls the probe from the main form. The form is composed of a menu bar, a tool bar and a status message bar. The menu bar provides options that allow the user to configure and run the probe. The tool bar provides options to configure the probe and the status bar displays the probes current status and/or any errors that may have been encountered. Error messages displayed in the status bar are also logged in the Log Form if logging is enabled.

The menu bar contains the following options:

File:

- Open Config File – Displays a open file dialog in which the user may navigate to and open the file contains a previous session's saved probed settings.
- Save As - Displays a save file dialog in which the user may specify where a probe settings configuration file may be saved.
- Exit – Shut down the application.

Edit:

- Modify Title String – Allows the user to specify the title string that appears in all sub-dialog's title bar. Helpful when running multiple probes.

Run/Stop:

- Run Probe Mgr – Running the probe with the current settings. This is an alternative to clicking the tool bar Run button.
- Stop Probe Mgr - Stop the probe. This is an alternative to clicking the tool bar Stop button

Upgrade:

- Upgrade – Upgrade one of four protocol specific FPAG configurations

Help:

- About – Display version numbers for the Probe Manager application and FPGA configuration.

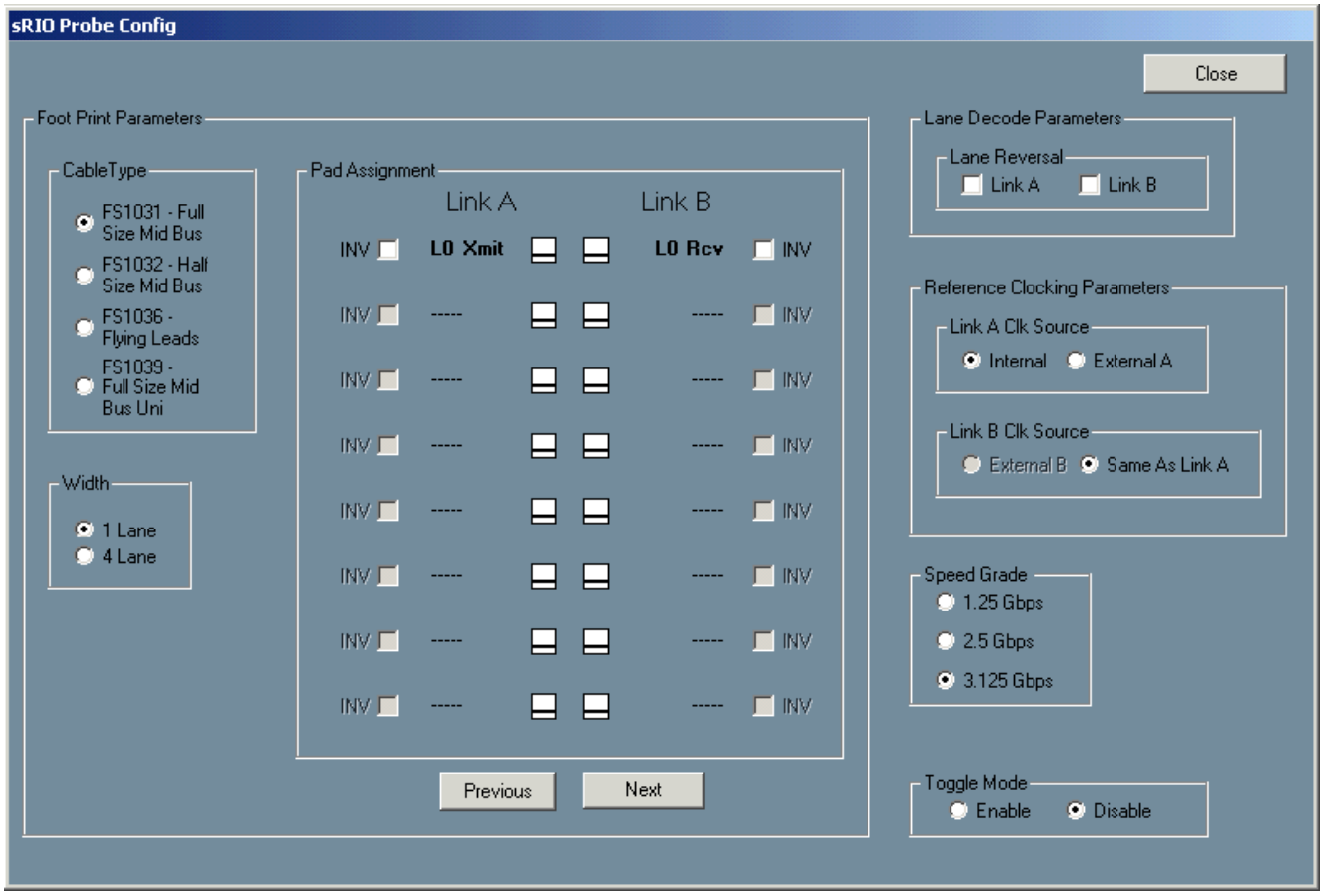
The application displays up to five sub-dialogs in a modeless manner. The sub-dialogs are used to configure the FS4400 probe.

The five sub-dialogs are:

- Probe Configuration – Covers the type of probe cable used and basic aspects of the link being probed.
- Packet Recognizers – Set up the 3 Packet Recognizers provided per Link, which may be used to specify packet header based triggering parameters.
- Filters – Allows the user to specify the types of packets to be filtered
- Log Entries – Run time probe status.

Probe Configuration

The Probe Configuration tab page provides the user with the ability to configure the probe and to monitor signal activity on each channel.



The functions provided on these forms include:

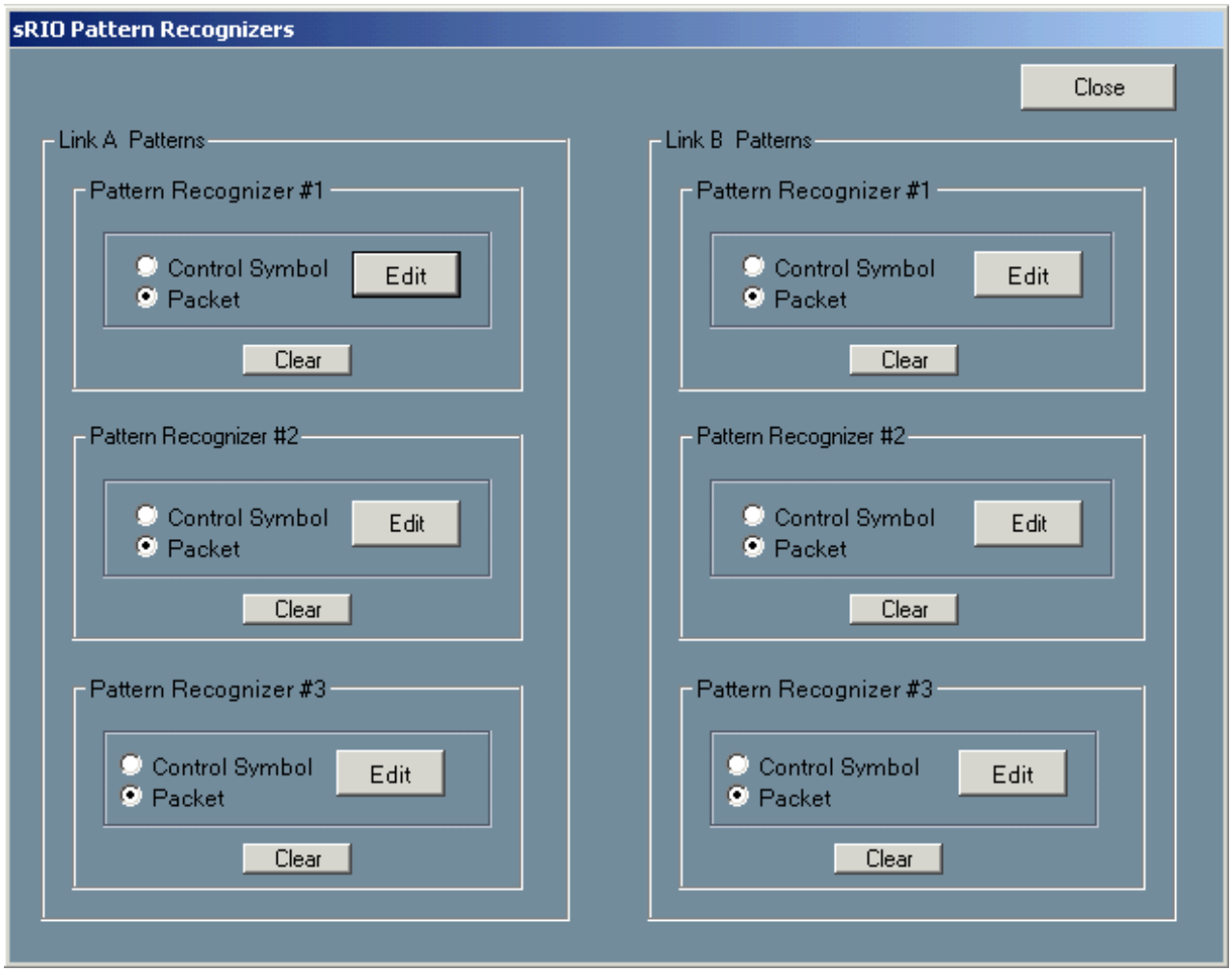
- Selection of the Probing Cable type, Link width, and Footprint shape. (Shape refers to the arrangement of lanes on the mid-bus probe pads; see the “sRIO Probing Design Guide for the FS4410” for more specific information.)
- Select sRIO bus width, either x1 or x4.
- The Pad Assignment graphic shows the assignment of logical lanes as a result of user selections, and also represents the physical layout of mid-bus pads. The FS4410 processes channels from the left column in link-processor A and from the right column in link-processor B.
- Next or Previous buttons scroll through the various types of currently supported pad assignments (see the “sRIO Probing Design Guide for the FS4410” for details of supported pad assignments).
- Lane Inversion can be selected on an individual channel basis by clicking the INV button associated with each lane.
- While the probe is stopped, signal activity indicators are provided on each channel. Signal presence is flagged by an up-down arrow symbol and the lack of signal is displayed by a flat horizontal line symbol.
- Selection of Lane Reversal on each link.

Probe Configuration, Continued

- Reference Clocking choices are to use the FS4410 Internal reference on both links (probed links must be running at one of the 3 nominal speed grades and have 100 PPM frequency accuracy) or use External Reference Clock signal(s) from the target platform, via the FS4410 external Ref. Clock cable.
- For sRIO external reference clocking, the expected frequency is the link bit rate divided by 20 (for example a speed grade 2 link runs at 2.5 Gbps and would have reference clock frequency of 125 MHz). If necessary, sRIO probing with a reference clock frequency divider of 25 is supported by the FS4410, contact FuturePlus Systems for details.
- Selection of external reference clock source for link B: “Same as A” (common clock, uses the Reference Clock A probe input), or “External B” (distinct clock, uses Reference Clock B probe input).
- Selection of Toggle mode. When activated, the logic analyzer pod signals, and the link status LEDs are toggled.

Packet Recognizers

This dialogue page provides the ability to setup the three 24-byte Pattern Recognizers provided on each link.

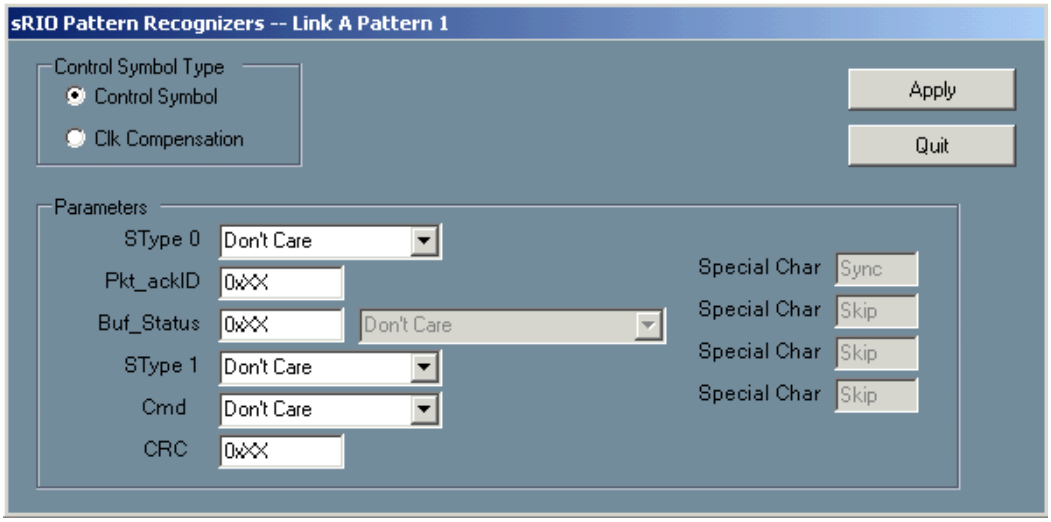


sRIO Pattern and Mask Dialog

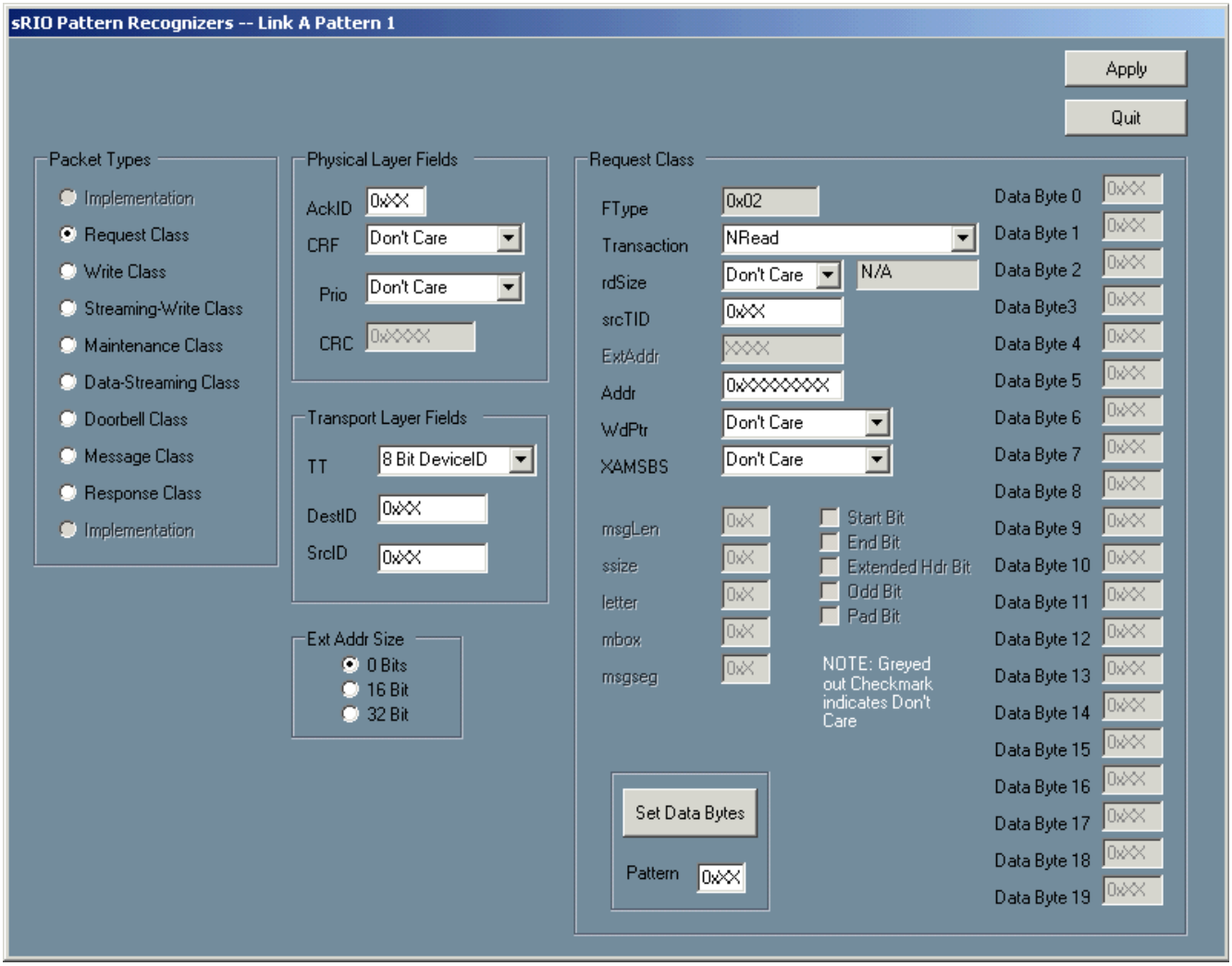
The Packet Recognizers dialog allows a user to specify the packet recognizer pattern.

The sRIO pattern and mask dialog allows the user to enter up to 6 patterns (3 on link A and 3 on link B).

The pattern is entered via a sub-dialog that is displayed after the user has clicked one of the six Edit buttons. There are two sub-dialog forms, one for control symbols and one for packets as shown below.



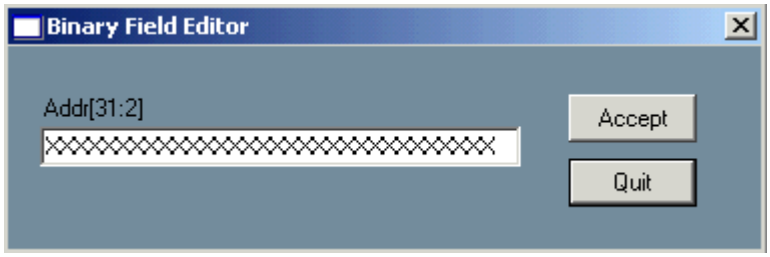
The Control Symbol pattern and mask dialogue.



The sRIO Packet pattern and mask dialogue.

The sRIO Control Symbol and Packet sub-dialog screens are designed such that the minimum numbers of fields are specified to form a valid packet. Fields displaying X's will be masked out. All reserved fields will be masked into the pattern.

Every field is validated as the user is entering the hex values. The user may enter any combination of X's and hex digits into each field. Each field may be edited in binary form by right clicking the mouse key, at which point the contents of the field are displayed in binary format in a separate window. When the user applies the binary values (by clicking the Accept button), the binary value is converted to a hex representation and displayed in the pattern dialog. Field Hex digits that are partially masked will be displayed with a "$" character.



Binary Editor Dialog

The packet recognition setups are created via sub-dialogs that are displayed whenever the user selects a packet type (via the radio buttons for each link pattern) and clicks the Edit button.

The pattern is edited if the user clicks the Apply button on the packet-specific sub-dialogue form. If edited, the packet type string is displayed in a light blue color.

Once edited, the pattern may be cleared by clicking the Clear button. This will inactivate the recognizer.

Pattern Recognizers are used to trigger the logic analyzer whenever a specific packet or ordered set pattern is encountered. Each Pattern recognizer outputs a PAT_REC flag to the logic analyzer that pulses high during the 1st state of each packet.

Pattern recognizers may also be used as filters.

The Pattern Recognizer examines the first 24 bytes of each packet. Recognizers are setup by the Probe Manager with a match pattern and a separate mask pattern, giving the user control over the comparison, bit by bit.

The probe must be stopped before editing patterns.

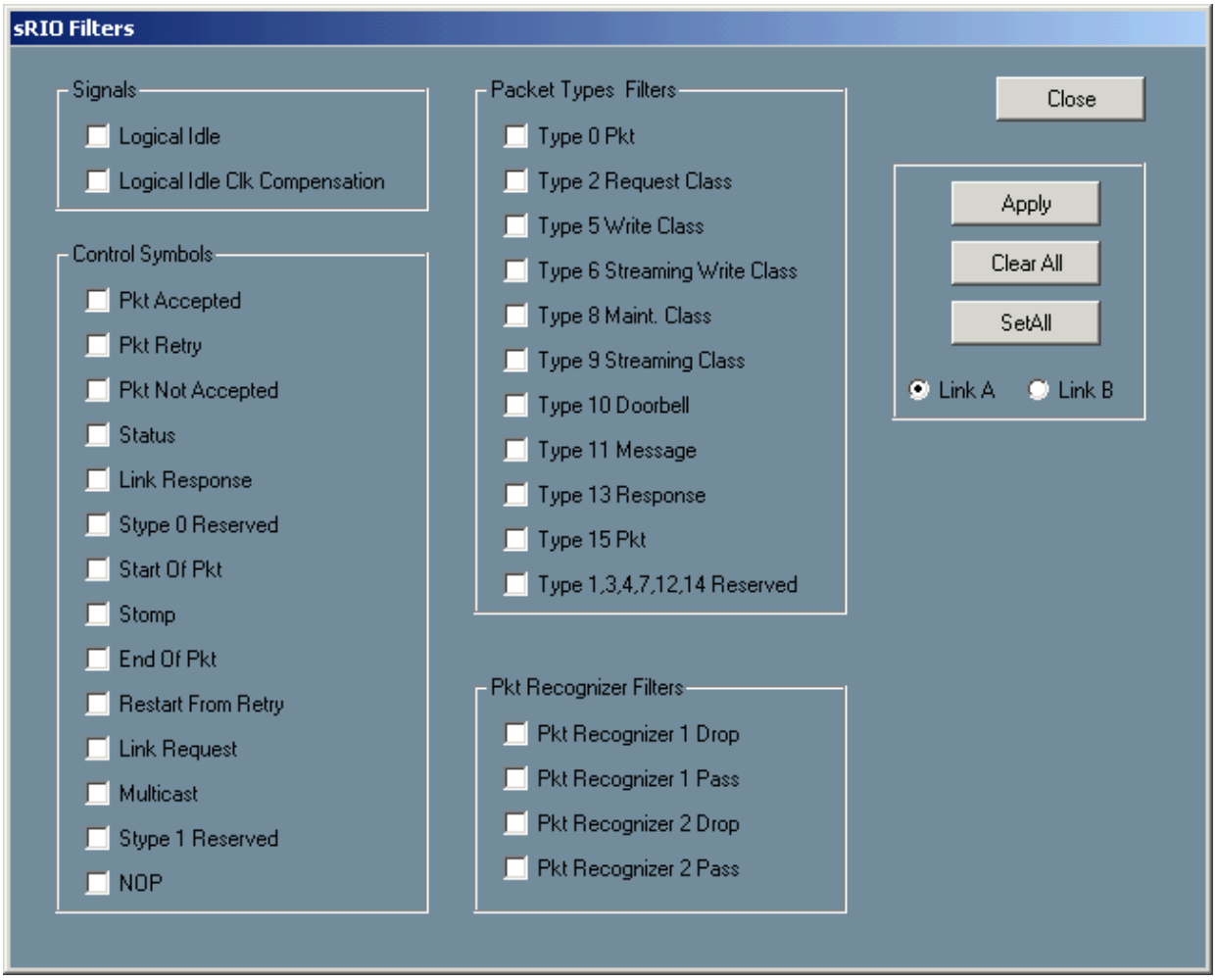
You must always restart the probe by pressing the green run button on the main window so the new values will be written to the probe hardware.

Filtering

The Filter dialogue page provides the user with a comprehensive suite of predefined filter functions to apply to either Link.

Filter types include signal state, Control symbol type, and Packet type.

Additionally, filters are provided to Pass or Drop packets that have been recognized by packet recognizers.



Filtering is done in real time by the FS4410 hardware.

Filtering out unwanted traffic such as Logical Idles can extend the storage capabilities of the logic analyzer.

Filtering out irrelevant bus traffic can help users focus on specific packets of interest.

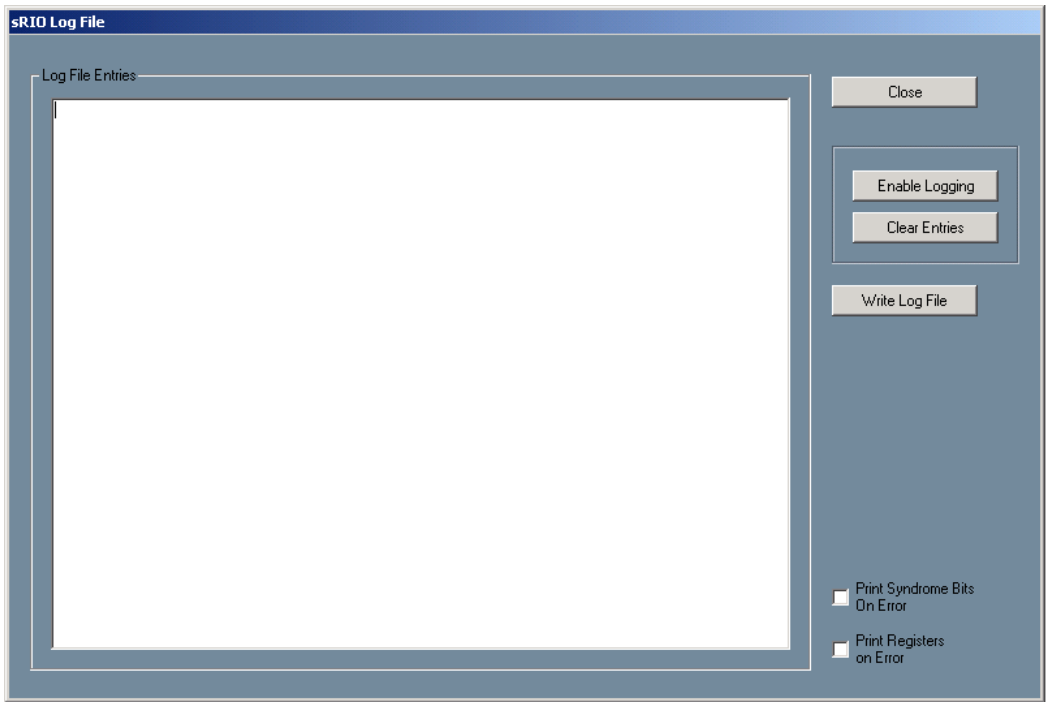
To filter out any particular traffic type, click on the appropriate box so an √ appears and click apply. You must restart the probe by pressing the green run button so the new values will be written to the probe hardware.

Use Link A and Link B buttons to switch to the other link's filter.

Filtering can also be done on any combination of packet header bits, via the Pattern Recognizers. The "Pkt Recognizer Drop" filter selections, when checked, filter out recognized packets. The "Pkt Recognizer Pass" filter selections, when checked, force the outputting of recognized packets to the analyzer and over-ride all other filters.

Log File

The status of the probe, while it is running, can be seen in this tab page.



Once started, logging continues even if the probe is stopped and started, or if the log window is closed and re-opened.

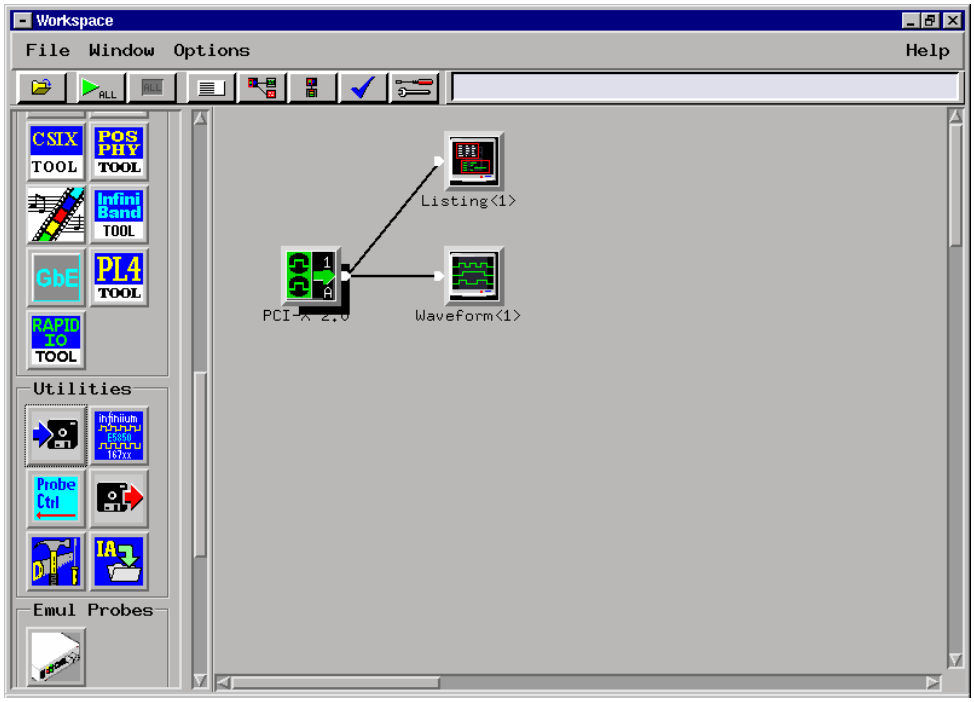
Once a probe has been stopped, the log entries can be written to a file of the user's choice by clicking the Write Log File button.

State Analysis

The sRIO Protocol Decode Software

This chapter explains how to use the FS4410 to perform state analysis. The configuration file sets up the format specification menu of the logic analyzer for compatibility with the output of the FS4410.

Loading the configuration file will automatically load the sRIO Protocol Decode software (FS4410) onto the workspace. If this does not happen then check to make sure that the sRIO decode software was properly installed.



Labels (8b)

Besides de-serializing the data stream for the logic analyzer, the FS4410 generates a number of identification and control bits that are used by the Protocol Decoder and logic analyzer. These are also available to the user and can be used as described below.

Please note that any changes to the Data or VAB labels in the logic analyzer's Format menu will prevent proper operation of the Protocol Decoder.

Field	Bits	Definition	Pod	Bits
VAB		Collection of probe-generated flags, listed below, defined for Inverse Assembler usage.		
DS	1	Default Store Flag 1= Store this state 0 = Discard	A4 (B4)	16
EOP	1	EOP = End-of-packet word (when = 1)		15
Error	1	1= This state includes an error		14
Error/Signal Code	4	Describes what type of error/signal event was detected. When Error = 1, this is an error code, see table. When Error = 0, this is a signal event code, see table.		13:10
Pat_Rec_3 Pat_Rec_2 Pat_Rec_3	3	1= Packet recognized (pulsed for one cycle at start of packet)		9:7
PSS[2:0] (Packet Sample State)	3	PSS[2] CS = Control Symbol (also used as an Event Code bit) PSS[1] SOP = Start of Packet PSS[0] INP = In Packet (asserted for all states of a packet) CS SOP INP EOP 0 0 0 0 Idle 1 0 0 0 Control Symbol (delimiter or non-delimiter) 0 1 1 0 Start Of Packet 0 0 1 0 In-packet words after the first word 1 0 1 0 Embedded Control Symbol 0 0 1 1 End Of Packet		6:4
Event_Code[5:0]	6	Describes what type of packet, control symbol, or idle detected. Code is held for duration of packet or control symbol. CS bit is used to discriminate Control Symbols versus Packets. In the label, CS bit is used as Event_Code[6]. See table.		3:0
			A3 (B3)	16:15
Data Present [3,2,1,0]	4	1= Corresponding lane data byte is present. 0= Data not present. "Not present" is due to lane spreading of x1 to 4 lane format.		14:11
LOS [3,2,1,0]	4	1= Corresponding lane Loss of Signal 0= Signal detect Logically named, reflects lane reverse status.		10:7
Lane 0 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		6
Lane 0 Control Flag	1	1=K character (control) 0= D character (data)		5
Lane 0 8b Data	8	Decoded 8b value		4:0
			A2 (B2)	16:14
Lane 1 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		13
Lane 1 Control Flag	1	1=K character (control) 0= D character (data)		12
Lane 1 8b Data	8	Decoded 8b value		11:4
Lane 2 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		3
Lane 2 Control Flag	1	1=K character (control) 0= D character (data)		2
Lane 2 8b Data	8	Decoded 8b value		1:0
			A1 (B1)	15:10
Lane 3 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		9
Lane 3 Control Flag	1	1=K character (control) 0= D character (data)		8
Lane 3 8b Data	8	Decoded 8b value		7:0

Event Code label definitions:

sRIO Event	CS	Event code
Unknown	0	000000
Signal Logical Idle	0	000101
Logical Idle Clock Compensation Sequence KRRR	0	000111
Control Symbol stype0 000 Packet-accepted	1	000xxx
Control Symbol stype0 001 Packet-retry	1	001xxx
Control Symbol stype0 010 Packet-not-accepted	1	010xxx
Control Symbol stype0 100 Status	1	100xxx
Control Symbol stype0 110 Link-response	1	110xxx
Control Symbol stype0 011, 101, 111 Reserved	1	011xxx
Control Symbol stype1 000 Start-of-packet	1	xxx000
Control Symbol stype1 001 Stomp	1	xxx001
Control Symbol stype1 010 End-of-packet	1	xxx010
Control Symbol stype1 011 Restart-from-retry	1	xxx011
Control Symbol stype1 100 Link-request	1	xxx100
Control Symbol stype1 101 Multicast-event	1	xxx101
Control Symbol stype1 110 Reserved	1	xxx110
Control Symbol stype1 111 NOP	1	xxx111
Packet Type 0 Implementation-defined	0	100000
Packet IO Type 2 Request Class	0	100010
Packet IO Type 5 Write Class	0	100101
Packet IO Type 6 Streaming Write	0	100110
Packet IO Type 8 Maintenance Class	0	101000
Packet Type 9 Data Streaming	0	101001
Packet Msg Type 10 Doorbell	0	101010
Packet Msg Type 11 Message	0	101011
Packet Type 13 Response	0	101101
Packet Type 15 Implementation-defined	0	101111
Packet Type 1,3,4,7,12,14 Reserved	0	100001
Filtered state, look at Error/Signal Code only	0	11xxxx

Error/Signal Code List

Errors and Signal Events are reported on every state in the Error/Signal Code field.

Event	ERROR	Error/Signal Event Code
No error or signal event	0	0000
Warning: ECS Overflow (Contact FPS)	0	1000
Warning: Ack ID Sequence	0	1001
Warning: Packet Cancelled	0	1010
Signal Event: Link Down	0	0001
Signal Event: Electrical Idle	0	0010
Signal Event: LOS in any Lane	0	0011
Signal Event: Link Alive	0	0100
Signal Event: Beacon (Lane 0 driven)	0	0101
Error: Invalid (10b Decode or Disparity error)	1	0001
Error: Alignment (“A” Column Check, x4 only)	1	0010
Error: Control Symbol CRC	1	0011
Error: Packet and Control Symbol Framing	1	0100
Error: Unexpected Control Character	1	0101
Error: Incorrect Idle Character	1	0111

All “Signal event” and “Error” types will be forced to output even during states that would normally be filtered out by probe hardware.

Signal Events:

Beacon indicates detection of the first signal driven on lane 0.

Link Alive indicates detection of first valid received data after link has been down.

Link Down indicates the receiver is failing to receive a signal.

LOS in any Lane indicates loss of signal in any active lane.

Electrical Idle indicates all active lanes have no signal.

Errors:

Invalid indicates 1 or more active lanes has an 8b10b disparity or invalid decode error.

Alignment indicates link is not de-skewed, based on “alignment column” check.

Control Symbol CRC indicates CRC check of control symbol failed.

Framing indicates improper sequence of control symbols and packet delimiters.

Unexpected Control asserts whenever a control character is found inside a packet.

Idle is asserted whenever anything other than a valid idle character (A, K, or R) is detected when the bus is not carrying packets or control symbols.

Warnings:

ECS overflow indicates the possibility that too many embedded control symbols were seen in a packet for full probe functionality. If this occurs, please contact FPS for details. We want to support a greater capability if needed.

Ack ID sequence indicates non-sequential values were seen for Ack-ID. This can happen as a result of packet re-tries.

Packet Cancelled indicates a packet was terminated prematurely.

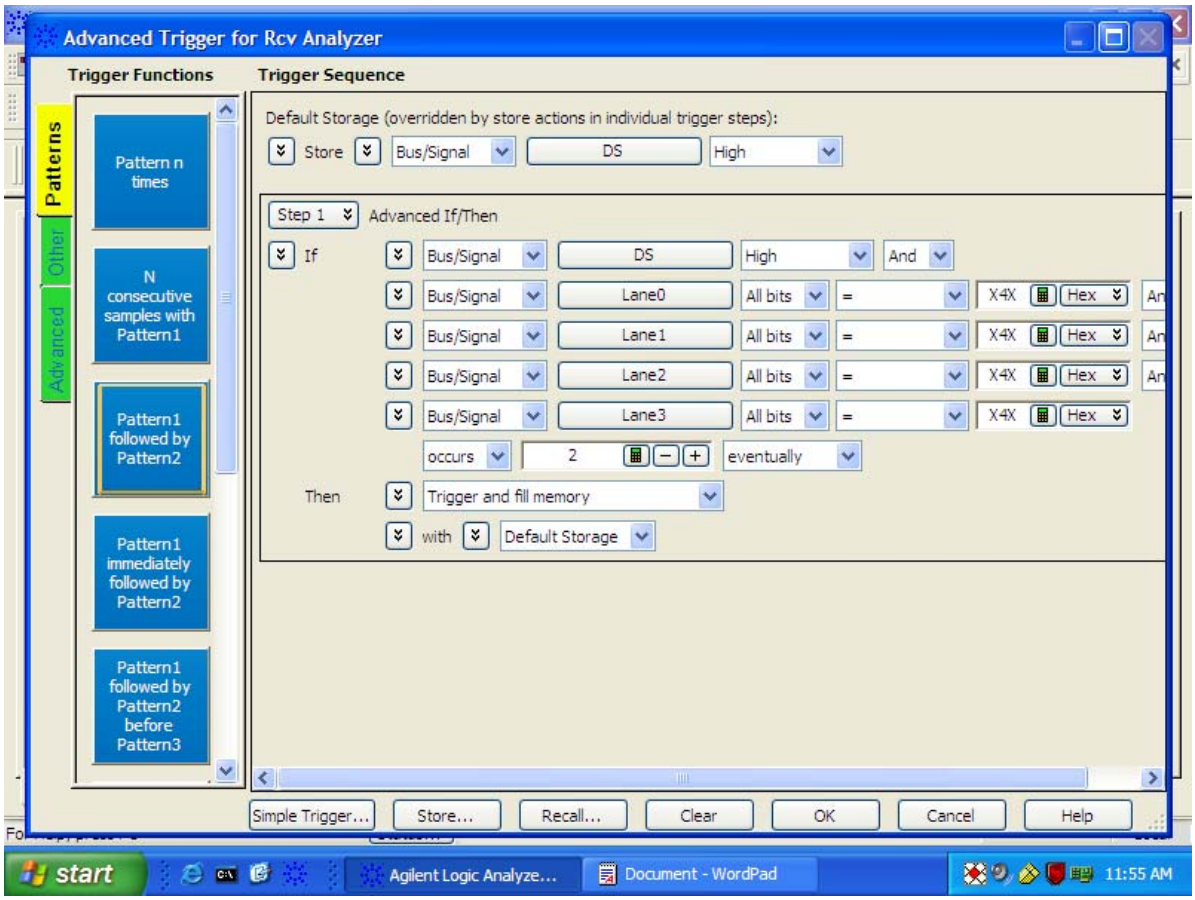
Labels (10b)

Besides de-serializing the data stream for the logic analyzer, the FS4410 in 10b Mode generates a number of status bits that are available to the user and can be used for triggering and analysis as described below.

Pre-defined Label	**No. of Bits**	**Definition/Usage**	**Logic Analyzer Pod** **10-bit, x1 mode** (use B pods for other link)	**Logic Analyzer Pod** **10-bit, x4 mode** (use B pods for other link)
Align Flag	1	1= Alignment of multi-lane link detected	NA	A4[4]
Any Invalid Error Flag	1	1= This state includes an 8b10b code error (either disparity error or decode error in any active lane)	A1[0]	A4[3]
LOS [3,2,1,0]	4	1= Corresponding lane Loss of Signal 0= Signal detect on lane (x4 mode only)	NA	A4[2:0] A3[16]
Any LOS	1	1= Loss of Signal detected in any active lane 0= Signal detected in all active lanes	A1[15]	A3[15]
Lane 0 Disparity Error	1	1= Lane 0 data has incorrect 8b10b disparity	A1[14]	A3[14]
Lane 0 Invalid Decode Error	1	1= Lane 0 data is not a valid 8b10b code	A1[13]	A3[13]
Lane0	10	Physical Lane 0 Data, 10-bit encoded	A1[12:3]	A3[12:3]
Lane 1 Disparity Error	1	1= Lane 1 data has incorrect 8b10b disparity	NA	A3[2]
Lane 1 Invalid Decode Error	1	1= Lane 1 data is not a valid 8b10b code	NA	A3[1]
Lane1	10	Physical Lane 1 Data, 10-bit encoded	NA	A3[0] A2[16:8]
Lane 2 Disparity Error	1	1= Lane 2 data has incorrect 8b10b disparity	NA	A2[7]
Lane 2 Invalid Decode Error	1	1= Lane 2 data is not a valid 8b10b code	NA	A2[6]
Lane2	10	Physical Lane 2 Data, 10-bit encoded	NA	A2[5:0] A1[15:12]
Lane 3 Disparity Error	1	1= Lane 3 data has incorrect 8b10b disparity	NA	A1[11]
Lane 3 Invalid Decode Error	1	1= Lane 3 data is not a valid 8b10b code	NA	A1[10]
Lane3	10	Physical Lane 3 Data, 10-bit encoded	NA	A1[9:0]

Triggering

The configuration files provide some logic analyzer based trigger set-ups that utilize the pre defined symbols described earlier.



Remember to always use DS for default storage, and use default store to fill memory.

The probe-generated Event Code field makes it easy to trigger on particular packet types, using the pre-defined symbols. When triggering on Event Code always qualify it with:

- DS =1 (for valid data)
- PSS[1] =1 (The start of packet flag).
- CS (Already included in pre-defined Event Code symbol definitions)

The probe-generated Packet Recognizer flags (Pat_Rec_3,2,1) make it easy to trigger on packets based on header or data bit patterns in the first 24 bytes of each packet. These flags are always valid, pulse once at the start of each recognized packet, and do not need any other bits to qualify them.

Acquiring Data

First, insure that the FS4410 probe is attached to it's external power supply and powered on, which would be indicated by a green Power On LED. Open up the Probe Manager software and insure the appropriate selections are made and applied, finally make sure that the probe is connected via the appropriate cable(s) to the target system.

Once connected, with the link active, open up the Probe Config window and select cable type, lane width, and reference clock options. Verify that lane activity indicators show activity at the correct lanes. Run the probe and observe the LEDs.

If a link's Signal LED is green but its Data LED is orange then there may be a need to select different options for lane width, lane reverse or lane inversion in the Probe Config window.

The FS4410 probe should show a green Signal LED of any Link being probed, as well as a green or dark data LED.

Configure the analyzer trigger menu to acquire serial RapidIO data. Select RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full; the trigger specification is TRUE or when you select STOP.

The logic analyzer will flash "Slow or Missing Clock" if it does not see the signal CLK toggling.

The logic analyzer will flash "Waiting in level 1" if the trigger specification has not been met.

Link status is communicated by a pair of LEDs as follows:

Signal LED State	Meaning
Dark	LOS (no signal on an active lane)
Red	RX Fault: Lost Lock on Ref Clock, Lost Synch on Data, FIFO over run or under run. See Log for more information.
Orange	Invalid Symbol or Disparity Error
Green	OK

Data LED State	Meaning
Red	FPGA Lost lock on clock(s). Probe needs to stop and run again.
Orange	Any Error: Invalid Symbol or Disparity Error, Align, Framing, Idle.
Green	OK, Data clocking into analyzer.
Dark	No Data (due to filtering or not running)

All transient events such as a single bit error, or a packet clocked into the analyzer, are stretched to short visible pulses on the LEDs.

Observing Link Start-up:

When using Internal Reference clock, the probe can be run at any time, before or after the target has powered up or link become active.

When using External Reference clock(s), the probe requires the target reference clock to be active before the probe is run.

In all cases, links may be re-started, and target systems may be re-booted, while the probe is running. This makes probing link initialization convenient.

Finding the Start of Signal Activity:

Set the analyzer to trigger on:

- "Event Code = Link Alive"

Another method is to trigger based on signal detection status (LOS = loss of signal).

- "Event Code = Beacon" (signal detected on lane 0)
- LOS[0] goes low (for 1-lane operation)
- LOS[3:0] goes low (all lanes signal detected in 4-lane operation)

Note: Some links startup cleanly (within 300 nS of de-assertion of LOS flag), but others do not. The probe itself can not achieve lock quickly until it receives a stable signal and a stable reference clock. Signal detection does not imply a valid serial data signal. Signal detection (LOS status) is delayed relative to link data capture.

Finding Stable SRIO Link Activity:

When a link is becoming active, set the analyzer to trigger on:

- "Event Code = Any Control Symbol"

Observing Link Activity :

The probe can follow links that go up and down:

- When a link is constantly transitioning back and forth between active and low power states, the Signal LEDs and the log file will report errors that can be ignored.

10b Mode Debug

The FS4410 requires an external reference clock connection when used in 10b mode.

The LEDs operate as described previously.

Note: When using the FS4410 in 10-bit Mode, the user must select a Logic Analyzer Configuration file based on the lane width of the link being probed. The user must also select the correct lane width in the Probe Config window.

The probe hardware does real-time, lane-based 8b10b error checking, lane deskew and lane deskew checking. There are no filters or pattern recognizers provided in 10b mode. Packets and ordered sets are detectable using the analyzer trigger capabilities, looking for the values listed below. There is no inverse assembler; however there are pre-defined symbols that make packet boundaries visible in the state listing.

The following are some useful 10b symbol definitions for serial RapidIO. These are available pre-loaded in the lane data symbol tables for convenient setup of triggers. Trigger on A, K, or R to find Idle data. Trigger on SC or PD to find any Control Symbol. Trigger on PD to find packet beginnings and ends.

Remember there are usually two different possible codes representing each character in 10-bit Mode.

			Value follows negative disparity				Value follows positive disparity		
K	K28.5		K+	0101_111100	17C		K-	1010_000011	283
SC	K28.0		SC+	0010_111100	0BC		SC-	1101_000011	343
PD	K28.3		PD+	1100_111100	33C		PD-	0011_000011	0C3
A	K27.7		A+	0001_011011	05B		A-	1110_100100	3A4
R	K29.7		R+	0001_011101	05D		R-	1110_100010	3A2

Verify Setup in 10-bit Mode:

To verify correct lane reverse settings when probing a 4-lane link, make sure the SC and PD characters appear on the leftmost lane.

To verify lane width settings, verify Data LED is green (checks for valid data on all lanes, and the successful de-skew of active lanes).

Finding the start of Signal Activity in 10-bit Mode:

Set the analyzer to trigger on signal detection status (LOS = loss of signal). Note this method can only be used when the probe is not setup for ASPM mode:

- ANYLOS goes low (all lanes signal detected)

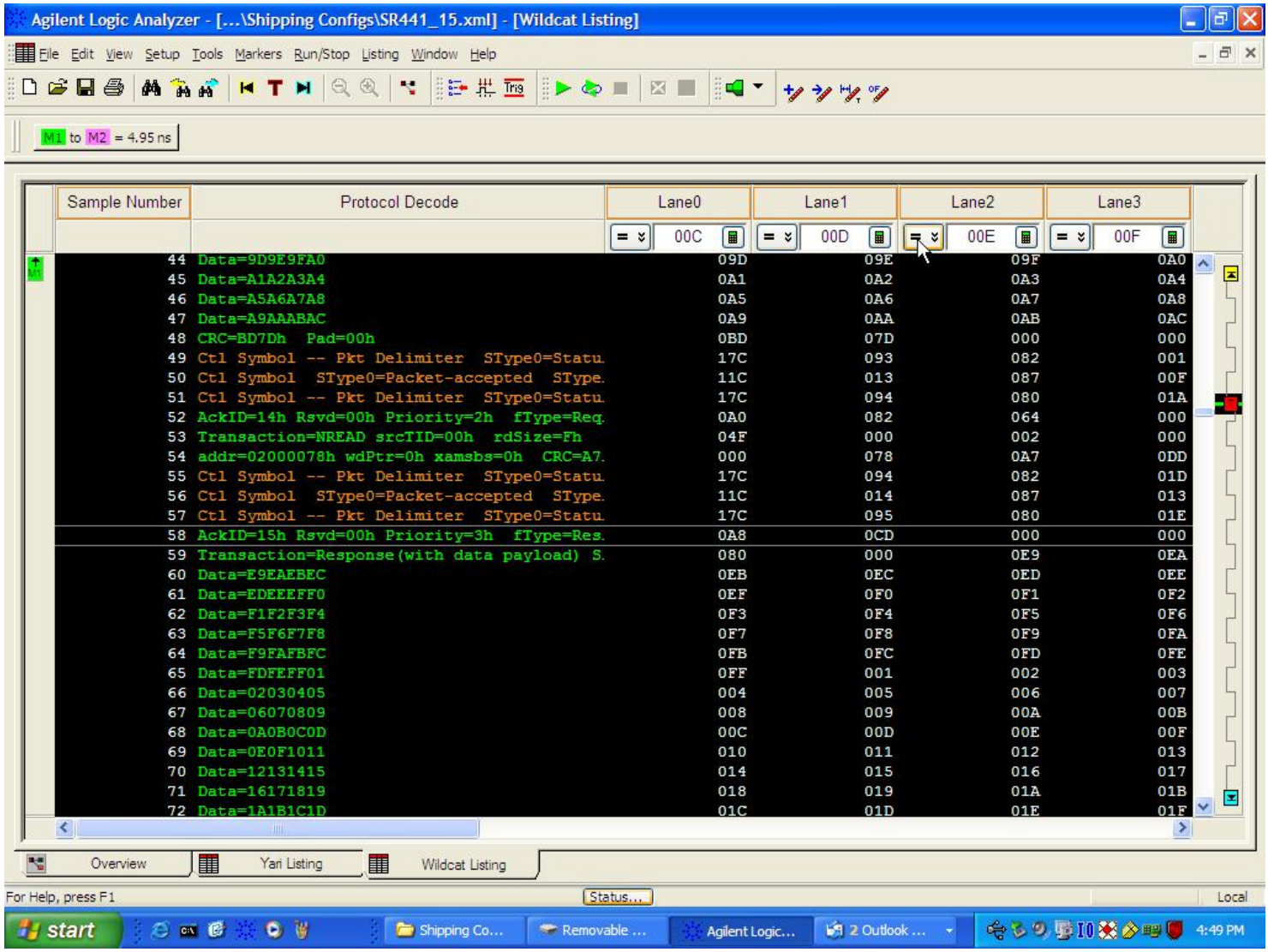
Note: Some links startup cleanly (within 300 nS of de-assertion of LOS flag), but others do not. The probe itself can not achieve lock quickly until it receives a stable signal and a stable reference clock. Signal detection does not imply a valid serial data signal. Signal detection (LOS status) is delayed relative to link data capture.

Note: When using an external reference clock, the probe requires it to be active before the probe will run. After the probe is running, it is permissable for the reference clock to be interrupted briefly by target or link re-start or re-boot.

Note: For faster 10-bit Mode acquisition of link data on a link as it is powering on, select ASPM mode in the probe manager GUI.

The State Listing Display

Captured data is as shown in the following figure. The below figure displays the protocol decode.


Agilent Logic Analyzer - [...\Shipping Configs\SR441_15.xml] - [Wildcat Listing]
File Edit View Setup Tools Markers Run/Stop Listing Window Help
M1 to M2 = 4.95 ns
Sample Number
Protocol Decode
Lane0
Lane1
Lane2
Lane3
00C
00D
00E
00F
44 Data=9D9E9FA0 09D 09E 09F 0A0
45 Data=A1A2A3A4 0A1 0A2 0A3 0A4
46 Data=A5A6A7A8 0A5 0A6 0A7 0A8
47 Data=A9AAABAC 0A9 0AA 0AB 0AC
48 CRC=BD7Dh Pad=00h 0BD 07D 000 000
49 Ctl Symbol -- Pkt Delimiter SType0=Statu. 17C 093 082 001
50 Ctl Symbol SType0=Packet-accepted SType. 11C 013 087 00F
51 Ctl Symbol -- Pkt Delimiter SType0=Statu. 17C 094 080 01A
52 AckID=14h Rsvd=00h Priority=2h fType=Req. 0A0 082 064 000
53 Transaction=NREAD srcTID=00h rdSize=Fh 04F 000 002 000
54 addr=02000078h wdPtr=0h xamsbs=0h CRC=A7. 000 078 0A7 0DD
55 Ctl Symbol -- Pkt Delimiter SType0=Statu. 17C 094 082 01D
56 Ctl Symbol SType0=Packet-accepted SType. 11C 014 087 013
57 Ctl Symbol -- Pkt Delimiter SType0=Statu. 17C 095 080 01E
58 AckID=15h Rsvd=00h Priority=3h fType=Res. 0A8 0CD 000 000
59 Transaction=Response(with data payload) S. 080 000 0E9 0EA
60 Data=E9EAEBEC 0EB 0EC 0ED 0EE
61 Data=EDEEEFF0 0EF 0F0 0F1 0F2
62 Data=F1F2F3F4 0F3 0F4 0F5 0F6
63 Data=F5F6F7F8 0F7 0F8 0F9 0FA
64 Data=F9FAFBFC 0FB 0FC 0FD 0FE
65 Data=FDFEFF01 0FF 001 002 003
66 Data=02030405 004 005 006 007
67 Data=06070809 008 009 00A 00B
68 Data=0A0B0C0D 00C 00D 00E 00F
69 Data=0E0F1011 010 011 012 013
70 Data=12131415 014 015 016 017
71 Data=16171819 018 019 01A 01B
72 Data=1A1B1C1D 01C 01D 01E 01F
Overview
Yari Listing
Wildcat Listing
For Help, press F1
Status...
Local
start
Shipping Co...
Removable ...
Agilent Logic...
2 Outlook ...
4:49 PM

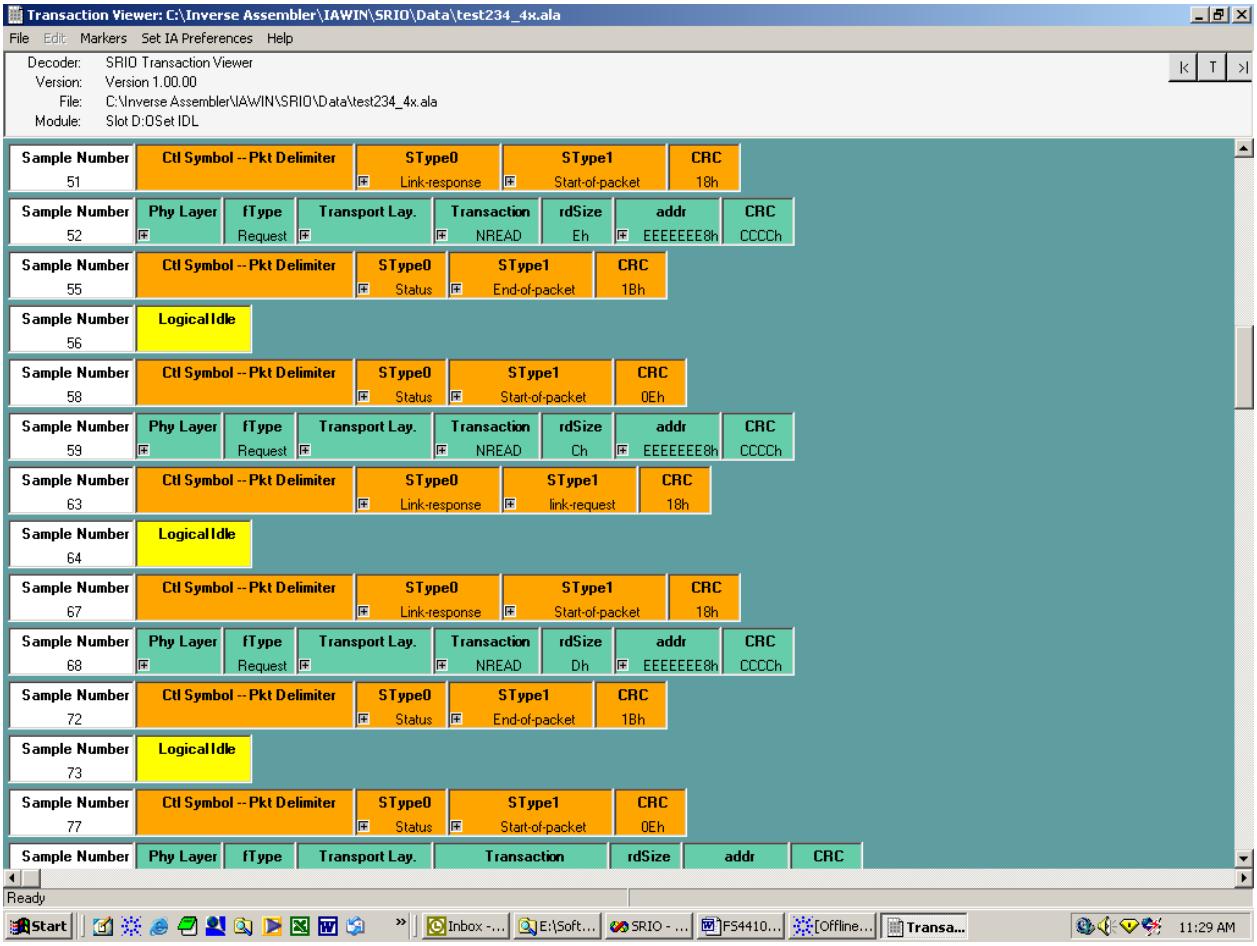
The FS4410 Decode Software will perform the following functions:

- Decode all sRIO command and cycle types
- Color code the transaction type. The colors used by the software are as follows:
  - Control Symbols: Orange
  - Packets: Green
  - Idle: White
  - Error: Red
  - Signal (Probe generated packets): Yellow
  - Unknowns: White

Transaction Viewer

The FS4410 Protocol Decoder is fully integrated with the FuturePlus Systems Transaction Viewer application.

This following figure is an example Transaction Viewer.


Transaction Viewer: C:\Inverse Assembler\IAWIN\SRIO\Data\test234_4x.ala
File Edit Markers Set IA Preferences Help
Decoder: SRIO Transaction Viewer
Version: Version 1.00.00
File: C:\Inverse Assembler\IAWIN\SRIO\Data\test234_4x.ala
Module: Slot D:OSet IDL
Sample Number 51 | Ctl Symbol -- Pkt Delimiter | SType0 Link-response | SType1 Start-of-packet | CRC 18h
Sample Number 52 | Phy Layer | fType Request | Transport Lay. | Transaction NREAD | rdSize Eh | addr EEEEEEE8h | CRC CCCCh
Sample Number 55 | Ctl Symbol -- Pkt Delimiter | SType0 Status | SType1 End-of-packet | CRC 1Bh
Sample Number 56 | Logical Idle
Sample Number 58 | Ctl Symbol -- Pkt Delimiter | SType0 Status | SType1 Start-of-packet | CRC 0Eh
Sample Number 59 | Phy Layer | fType Request | Transport Lay. | Transaction NREAD | rdSize Ch | addr EEEEEEE8h | CRC CCCCh
Sample Number 63 | Ctl Symbol -- Pkt Delimiter | SType0 Link-response | SType1 link-request | CRC 18h
Sample Number 64 | Logical Idle
Sample Number 67 | Ctl Symbol -- Pkt Delimiter | SType0 Link-response | SType1 Start-of-packet | CRC 18h
Sample Number 68 | Phy Layer | fType Request | Transport Lay. | Transaction NREAD | rdSize Dh | addr EEEEEEE8h | CRC CCCCh
Sample Number 72 | Ctl Symbol -- Pkt Delimiter | SType0 Status | SType1 End-of-packet | CRC 1Bh
Sample Number 73 | Logical Idle
Sample Number 77 | Ctl Symbol -- Pkt Delimiter | SType0 Status | SType1 Start-of-packet | CRC 0Eh
Sample Number | Phy Layer | fType | Transport Lay. | Transaction | rdSize | addr | CRC
Ready
Start
Inbox -...
E:\Soft...
SRIO - ...
F54410...
[Offline...
Transa...
11:29 AM

The Transaction Viewer is a powerful tool that allows the user to view data captured with the FS4410 in a graphical environment that presents the information by Transaction as opposed to State.

This tool is fully integrated with State Listing on the 16900 and allows marker and trigger settings to be shared between the Protocol Decoder and the Transaction Viewer.

The Transaction Viewer itself is a separate application that needs to be downloaded from the FuturePlus Systems website: www.futureplus.com. The user manual for the Transaction Viewer is also separate and can be found either on the FuturePlus Systems Documentation CD on the FuturePlus Systems website.

The screen listed above displays the same set of transactions that are contained in the previous sections' IA trace protocol decode screen

As you can see, the level of detail has been brought up to the transactional level with the effect of allowing the new tool to show a much greater range of decoded trace states.

General Information

This chapter provides additional reference information including the characteristics and signal connections for the FS4410 probe.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the FS4410 probe.

Standards Supported

Serial RapidIO, Revision 1.3

Power Requirements

100-240VAC, 2 amps.

Logic Analyzer Required

Agilent 16715/6/7/9 or 16750/1/2 installed in the 16700A or 16700B mainframe. 16753 cards or better are recommended. 168x/9x and 1690x.

Number of Probes Used

The State Adapter Probe interface uses 8 cable headers of either the 40 pin or 80 pin type.

Logic Analyzer State Clock Frequency

62.5, 125, and 156MHz for x1 sRIO Protocol Analysis or 125, 250, 312.5MHz for x4.

In 10b mode: 125, 250, 312.5MHz (for x1 or x4)

Environmental Temperature

Non operating: -40 to +75 degrees C (-40 to +167 degrees F)

Altitude

Operating: 4,6000m (15,000 ft)

Non operating: 15,3000m (50,000 ft)

Humidity

Up to 90% non condensing. Avoid sudden, extreme temperature changes which would cause condensation on the FS4410 module.

Testing and Troubleshooting

There are no automatic performance tests or adjustments for the FS4410 module. If a failure is suspected in the FS4410 module contact the factory or your FuturePlus Systems authorized distributor.

Servicing

The repair strategy for the FS4410 is module replacement. However, if parts of the FS4410 module are damaged or lost contact the factory for a list of replacement parts.

Signal Connections

The FS4410 contains 8 90 pin Samtec pod connections and a duplicate 8 40 pin pod connections for use with older logic analyzer modules. These are wired in parallel and both sets of connections are always driven by the FS4410

The following is the pinout configuration of the connectors, (repeat for 2nd link-direction – "B" pods)

LAI Bit Definitions for a Single Direction x1, x4 Link

(4 Pods, 1 machine)

Field	Bits	Definition	Pod	Bits
Default Store Flag	1	1= Store this state 0 = Discard	A4 (B4)	16
EOP (helper bit)	1	EOP = End-of-packet word (when = 1)		15
Error	1	1= This state includes an error		14
Error/Signal Code	4	Describes what type of error/signal event was detected When Error = 1, this is an error code When Error = 0, this is a signal event code		13:10
Packet Recognizer	3	1= Packet recognized (pulsed for one cycle at start of packet)		9:7
Packet Sample State	3	[6] CS = Control Symbol (also used as an Event Code bit) [5] SOP = Start of Packet [4] INP = In Packet (asserted for all states of a packet) CS SOP INP EOP 0 0 0 0 Idle 1 0 0 0 Control Symbol (delimiter or non-delimiter) 0 1 1 0 Start Of Packet 0 0 1 0 In-packet words after the first word 1 0 1 0 Embedded Control Symbol 0 0 1 1 End Of Packet		6:4
Event Code	6	Describes what type of packet, control symbol, or idle detected. Code is held for duration of packet or control symbol. CS bit is used to discriminate Control Symbols and Packets.		3:0
			A3 (B3)	16:15
Data Present [3,2,1,0]	4	1= Corresponding lane data byte is present. 0= Data not present. "Not present" is due to lane spreading of x1 to 4 lane format.		14:11
LOS [3,2,1,0]	4	1= Corresponding lane Loss of Signal 0= Signal detect Logically named, reflects lane reverse status.		10:7
Lane 0 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		6
Lane 0 Control Flag	1	1=K character (control) 0= D character (data)		5
Lane 0 8b Data	8	Decoded 8b value		4:0
			A2 (B2)	16:14
Lane 1 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		13
Lane 1 Control Flag	1	1=K character (control) 0= D character (data)		12
Lane 1 8b Data	8	Decoded 8b value		11:4
Lane 2 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		3
Lane 2 Control Flag	1	1=K character (control) 0= D character (data)		2
Lane 2 8b Data	8	Decoded 8b value		1:0
			A1 (B1)	15:10
Lane 3 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity or code violation.		9
Lane 3 Control Flag	1	1=K character (control) 0= D character (data)		8
Lane 3 8b Data	8	Decoded 8b value		7:0

The clock is on A1 bit 17 (B1 bit 17).

LAI Bit Definitions for a Single Direction x4 Link 10b mode

(4 Pods, 1 machine)

Field	Bits	Definition	Pod	Bits
Unused	12	Set to 0	A4	16:5
Align Flag	1	1 = Alignment of multi-lane link detected	B4	4
Any Invalid Error Flag	1	1 = This state includes a 10B code error (disparity or decode) in any active lane.		3
LOS[3,2,1,0]	4	1 = Corresponding lane Loss of Signal. 0 = Signal detect.		2:0
			A3	16
ANY LOS	1	1 = Any Lane Loss of Signal 0= Signal detect on all active lanes	B3	15
Lane 0 Disparity Error	1	1 = Lane data is the wrong 10B disparity		14
Lane 0 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		13
Lane 0 10B Data	10	Encoded 10b value		12:3
Lane 1 Disparity Error	1	1 = Lane data is the wrong 10B disparity		2
Lane 1Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		1
Lane 1 10B Data	10	Encoded 10b value		0
			A2	16:8
Lane 2 Disparity Error	1	1 = Lane data is the wrong 10B disparity	B2	7
Lane 2 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		6
Lane 2 10B Data	10	Encoded 10b value		5:0
			A1	15:12
Lane 3 Disparity Error	1	1 = Lane data is the wrong 10B disparity	B1	11
Lane 3 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		10
Lane 3 10B Data	10	Encoded 10b value		9:0

The clock is on A1 bit 16 (B1 bit 16).

LAI Bit Definitions for a Single Direction X1 10b mode Link

(1 Pod, 1 machine) (repeat for 2nd link-direction)

Field	Bits	Definition	Pod	Bits
ANY LOS	1	1 = Any Lane Loss of Signal 0= Signal detect on all active lanes	A1 B1	15
Lane 0 Disparity Error	1	1 = Lane data is the wrong 10B disparity		14
Lane 0 Invalid Decode Error	1	1 = Lane data is an invalid 10B decode		13
Lane0	10	Encoded 10b value		12:3
Unused	2	Set to 0		2:1
Any Invalid Error Flag	1	1 = This state includes a 10B code error (disparity or decode) in any active lane.		0

The clock is on A1 bit 16 (B1 bit 16).